nRF54L05

Revision 1

Errata

v1.0

NORDIC® SEMICONDUCTOR

Contents

1 nRF54L05 Revision 1 Errata

This Errata document contains anomalies and configurations for the nRF54L05 SoC, Revision 1 (QFAA-A00).

2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF54L05 Revision 1 v1.0	18.03.2025	• Added: No. 6. “Spectrum of transmitted signal is not optimal for 802.15.4” • Added: No. 39. “Device can behave erratically after XOSTART” • Added: No. 41. “Sensitivity is degraded on n*32 MHz channels” • Added: No. 44. “DMA.RX.AMOUNT is not updated with bytes count after match event” • Added: No. 47. “Device resets while debugging in System OFF mode” • Added: No. 48. “RESETREAS register might show an additional wakeup source after reset” • Added: No. 49. “First bits of on-air packet are not correct”
nRF54L05 Revision 1 v0.8	08.01.2025	• Added: No. 1. “MAC error is returned if MDATA size is slightly larger than MLEN” • Added: No. 7. “RXD.AMOUNT is not updated after RXFLUSH if FIFO is empty” • Added: No. 8. “Wrong data is transmitted on MOSI” • Added: No. 16. “Cleared EVENTS are triggered again on the next CNT0 event” • Added: No. 17. “Bus faults during hibernate save sequence are ignored” • Added: No. 18. “Subsequent VPR hibernate sleeps might fail to save ra” • Added: No. 20. “RADIO payload is not transmitted” • Added: No. 21. “MOSI line toggles after transmission ends” • Added: No. 22. “EVENTS_COMPARE[n] event is not generated” • Added: No. 23. “READY and READYNEXT events are generated when CPU wakes up” • Added: No. 24. “EVENT_COMPARE is not generated when using PPI” • Added: No. 25. “EVENT_COMPARE[n] is not generated” • Added: No. 26. “PPIB between domains uses wrong security attribution” • Added: No. 30. “GRTC operates incorrectly at low temperature” • Added: No. 31. “Current consumption is higher than expected in sleep” • Added: No. 32. “Regulators have incorrect trims” • Added: No. 37. “Current consumption might increase after pin reset or power cycle”

3 New and inherited anomalies

The following anomalies are present in Revision 1 of the nRF54L05 SoC.

ID	Module	Description	New in Revision 1
1	CCM	MAC error is returned if MDATA size is slightly larger than MLEN	X
6	RADIO	Spectrum of transmitted signal is not optimal for 802.15.4	X
7	UARTE	RXD.AMOUNT is not updated after RXFLUSH if FIFO is empty	X
8	SPIM	Wrong data is transmitted on MOSI	X
16	VPR	Cleared EVENTS are triggered again on the next CNT0 event	X
17	VPR	Bus faults during hibernate save sequence are ignored	X
18	VPR	Subsequent VPR hibernate sleeps might fail to save ra	X
20	CLOCK	RADIO payload is not transmitted	X
21	SPIM	MOSI line toggles after transmission ends	X
22	TIMER	EVENTS_COMPARE[n] event is not generated	X
23	RRAMC	READY and READYNEXT events are generated when CPU wakes up	X
24	TIMER	EVENT_COMPARE is not generated when using PPI	X
25	TIMER	EVENT_COMPARE[n] is not generated	X
26	DPPI	PPIB between domains uses wrong security attribution	X
30	CLOCK, GRTC	GRTC operates incorrectly at low temperature	X
31	POWER	Current consumption is higher than expected in sleep	X
37	POWER	Current consumption might increase after pin reset or power cycle	X
39	CLOCK	Device can behave erratically after XOSTART	X
41	RADIO	Sensitivity is degraded on n*32 MHz channels	X
44	EASYDMA	DMA.RX.AMOUNT is not updated with bytes count after match event	X
47	POWER	Device resets while debugging in System OFF mode	X
48	RESET	RESETREAS register might show an additional wakeup source after reset	X
49	RADIO	First bits of on-air packet are not correct	X

Table 1: New and inherited anomalies

3.1 [1] CCM: MAC error is returned if MDATA size is slightly larger than MLEN

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

A MAC error is generated.

Conditions

The MDATA size is larger than MLEN by 1 or a few bytes.

Consequences

Payload is lost due to MAC error.

Workaround

Use MLEN or a significantly bigger value than MLEN for the size of the MDATA job. For example, use mdata.size=1000 when a payload length in the range from 1 to 251 bytes is expected, but the exact payload length is not known beforehand.

3.2 [6] RADIO: Spectrum of transmitted signal is not optimal for 802.15.4

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

The FCC restricted band edge requirement might not be met for 2405 MHz and 2480 MHz.

Conditions

The radio is operating in the IEEE 802.15.4 mode at TX output power level above 0 dBm.

Consequences

The limit for emissions outside of the band might be violated for 2405 MHz and 2480 MHz.

Workaround

Perform the following register write immediately after setting RADIO.MODE to Ieee802154_250Kbit:

```
*(volatile uint32_t *) 0x5008A810 = 2;
```

The workaround can be applied to all channels and output powers.

3.3 [7] UARTE: RXD.AMOUNT is not updated after RXFLUSH if FIFO is empty

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

Wrong number of transferred bytes is reported.

Conditions

During the handling of the RXTO event, FLUSHRX is performed and the number of transferred bytes does not exceed MAXCNT.

Consequences

UARTE operations are unreliable.

Workaround

Apply the following workaround:

```
/* Setup buffer to which data can be flushed. */
UARTE->DMA.RX.PTR = buf;
UARTE->DMA.RX.MAXCNT = 5;
/* Clear READY. Needed for the workaround. */
UARTE->EVENTS_DMA.RX.READY = 0;
UARTE->EVENTS_DMA.RX.END = 0;
/* Trigger flushing. */
UARTE->TASKS_FLUSHRX = 1;
/* Wait until flushing is done. */
while (UARTE->EVENTS_DMA.RX.END == 0);
/* If READY event is set then use AMOUNT value else FIFO was empty.
 * If not for the PAN, AMOUNT could be read without checking READY event. */
fifo_cnt = (UARTE->EVENTS_DMA.RX.READY == 1) ? UARTE->DMA.RX.AMOUNT : 0;
```

This workaround clears the EVENTS_DMA.RX.READY before starting the flushing, and reads EVENTS_DMA.RX.READY after the flushing to determine if FIFO had data and DMA.RX.AMOUNT has valid data.

3.4 [8] SPIM: Wrong data is transmitted on MOSI

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

Wrong data is sampled.

Conditions

SPIM is configured with CPHA to 0, PRESCALER is larger than 2, and the first transmitted bit is 1.

Consequences

Wrong data is transmitted.

Workaround

Use the following workaround if PRESCALER is larger than 2.

Before triggering SPIM.TASKS_START, complete the following steps:

1. Set SPIM.IFTIMING.CSNDUR = SPIM.PRESCALER / 2 + 1 or any larger value.
2. Write value 0x82 to the corresponding SPIM instance address offset 0xc84.

When SPI.EVENTS_STARTED has been generated, write value 0x00 to the corresponding SPIM instance address offset 0xc84.

3.5 [16] VPR: Cleared EVENTS are triggered again on the next CNT0 event

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

TRIGGERED events are triggered again on the following CNT0 event.

Conditions

A TRIGGERED event is set with CSR and cleared.

Consequences

APB cannot be used to properly clear events if CNT0 is used.

Workaround

Set up a VPR TASK which triggers an interrupt in the VPR to clear the relevant VEVENTS bits through a CSR write. Do not use VPR EVENTS to trigger interrupts. Alternatively, use DPPI from the VPR to the EGU to interrupt the CPU.

3.6 [17] VPR: Bus faults during hibernate save sequence are ignored

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

Bus error responses during hibernate save are ignored.

Conditions

A bus fault occurs during the hibernate save sequence.

Consequences

The VPR CPU behavior is undefined.

Workaround

Ensure that the VPR context save memory (VPRSAVEADDR) is accessible by VPR.

3.7 [18] VPR: Subsequent VPR hibernate sleeps might fail to save ra

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

GPR x1 (ra) is not updated.

Conditions

VPR enters sleep in VPR hibernate mode multiple times without powering down.

Consequences

The VPR application might misbehave.

Workaround

After waking up from sleep in VPR hibernate mode, issue an APB write with VPR anywhere inside its own RTP or CPUCTRL peripheral address range.

3.8 [20] CLOCK: RADIO payload is not transmitted

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

Preamble is correctly transmitted but all following payloads are not transmitted.

Conditions

CPU and peripherals in MCU power domain are sleeping when RADIO starts transmitting.

Consequences

Transmission is corrupted.

Workaround

Before triggering RADIO.TASKS_RXEN or RADIO.TASKS_TXEN, trigger POWER.TASKS_CONSTLAT.

When disabling RADIO, trigger POWER.TASKS_LOWPWR.

The workaround might increase current consumption.

3.9 [21] SPIM: MOSI line toggles after transmission ends

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

One additional transition appears on the MOSI line at the end of the transmission when the clock has stopped toggling.

Conditions

SPIM00 or SPIM02 is being used with SPI mode 0. The first transmitted bit in the final byte is 1.

Consequences

None.

Workaround

None.

3.10 [22] TIMER: EVENTS_COMPARE[n] event is not generated

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

The generation of the EVENTS_COMPARE[n] does not occur.

Conditions

TIMER has been used in counter mode, counted to 1, and cleared. The power domain associated with TIMER is powered down. TIMER is then used in timer mode, and CC[n] is 1.

Consequences

The EVENT is missed.

Workaround

Apply one of the following workarounds:

- Do not use CC=1.
- Use SHORT register to stop and clear TIMER.
- Use PPI and START and CLEAR tasks at the same time.

3.11 [23] RRAMC: READY and READYNEXT events are generated when CPU wakes up

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

READY and READYNEXT are set when the CPU is waking up.

Conditions

The CPU wakes up.

Consequences

READY and READYNEXT cannot be relied on immediately after CPU wakes up.

Workaround

Do not use READY or READYNEXT in combination with CPU sleep.

3.12 [24] TIMER: EVENT_COMPARE is not generated when using PPI

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

The PPI enabled by PUBLISH_COMPARE[n] is not generated.

Conditions

DPPI channel is using TIMER EVENTS_COMPARE as an event with CC[n]=1.

Consequences

The PPI is missing.

Workaround

Apply one of the following workarounds:

- Do not use CC=1.
- Use SHORT register to stop and clear TIMER.
- Use PPI and START and CLEAR tasks at the same time.

3.13 [25] TIMER: EVENT_COMPARE[n] is not generated

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

EVENTS_COMPARE[n] is not generated for TIMER00 or TIMER10.

Conditions

The TIMER is configured with Timer mode and CC[n]=x+1, where x is the internal Counter value after TIMER is stopped. The TIMER is started once and then stopped with internal Counter at x. The power domain associated with the TIMER is powered down. The TIMER is started through PPI.

Consequences

The EVENT is missed.

Workaround

Apply one of the following workarounds for TIMER00 or TIMER10:

- Write TIMER base + 0x010 = 1 after STOP and before next START task.
- Trigger DPPI task at subscribe register TIMER base + 0x090 after stop and before next start.

This clears the counter.

Alternatively, the following workaround can be used for TIMER00:

Start timer with write to TASKS_START.

3.14 [26] DPPI: PPIB between domains uses wrong security attribution

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

PPIB channel security does not use the correct setting.

Conditions

DPPIC channels are configured with different S/NS security, and the PPIB channel subscribes to a DPPIC index different from the PPIB channel index.

Consequences

PPIB channels are blocked.

Workaround

Configure PPIB subscribe and publish to use the DPPIC channel of matching index, for example use DPPIC channel 0 for PPIB channel 0.

3.15 [30] CLOCK, GRTC: GRTC operates incorrectly at low temperature

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

GRTC drifts in frequency at low temperature.

Conditions

The system is using HFINT.

Consequences

Applications with real-time requirements can behave unexpectedly.

Workaround

A workaround is implemented in nRF Connect SDK 2.8.0 when MPSL is used.

3.16 [31] POWER: Current consumption is higher than expected in sleep

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

The device might have higher than expected current consumption while it is sleeping in System ON mode. Typically, the consumption is 1.2 µA instead of 0.6 µA without any RAM retained.

Conditions

The device is in System ON mode with the CPU and all peripherals in IDLE state.

Consequences

The device has higher current consumption than expected.

Workaround

Perform the following operations during device start-up and before enabling DC/DC:

```
*(uint32_t*)0x50120624 = 20 | 1<<5;
*(uint32_t*)0x5012063C &= ~(1<<19);
```

3.17 [37] POWER: Current consumption might increase after pin reset or power cycle

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

Current consumption is higher than expected in System OFF mode.

Conditions

The device is entering System OFF mode too soon after a pin reset or power cycle.

Consequences

Current consumption is higher than expected.

Workaround

Apply the following workaround:

1. Perform the following code: *(volatile uint32_t *) 0x5005340C =1;
2. Ensure that 40 CPU cycles are executed before entering System OFF mode.

3.18 [39] CLOCK: Device can behave erratically after XOSTART

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

The device behaves erratically or becomes unresponsive.

Conditions

The XOSTART task is triggered when the PLLSTART task is not triggered and CPU is sleeping.

Consequences

Peripherals outside the MCU domain can behave erratically.

Workaround

Trigger TASKS_PLLSTART before TASKS_XOSTART is triggered and trigger TASKS_PLLSTOP after TASKS_XOSTOP is triggered. Current consumption might increase depending on the use case.

3.19 [41] RADIO: Sensitivity is degraded on n*32 MHz channels

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

Sensitivity is reduced on the 2432 MHz and 2464 MHz channels.

Conditions

The radio is set to a receive channel which is an integer multiplier of the 32 MHz reference frequency.

Consequences

- Sensitivity is degraded on 1 Mbps BLE, 2 Mbps BLE, nRF1M, and nRF2M by approximately 2 dB.
- Sensitivity is degraded on nRF4M by approximately 2 dB on channels 2402, 2430, 2432, 2334, 2462, 2464, and 2466.
- Sensitivity is degraded on BLR125K by approximately 4 dB.
- Sensitivity is degraded on IEEE 802.15.4 by approximately 2 dB in the 2465 MHz RX frequency.

3.20 [44] EASYDMA: DMA.RX.AMOUNT is not updated with bytes count after match event

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

When a MATCH event is generated, DMA.RX.AMOUNT does not reflect the position of the character in memory.

Conditions

TWIM, SPI, or UART is used in RX mode with match candidates set up and match filter enabled.

Consequences

DMA.RX.AMOUNT cannot be used as a reliable offset with DMA.RX.PTR to find the matching character in memory.

3.21 [47] POWER: Device resets while debugging in System OFF mode

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

The device is not responsive to the debugger and resets during debug operations.

Conditions

The device is in emulated System OFF mode and at temperature above 98°C or has power-intensive operations in firmware immediately after the line putting it into System OFF mode.

Consequences

Debug access is unstable.

Workaround

After a failed attempt, retry debug operations.

3.22 [48] RESET: RESETREAS register might show an additional wakeup source after reset

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

RESETREAS wakeup field has an incorrect value.

Conditions

A wakeup source is active during a reset.

Consequences

Reset reason might lead to an incorrect assumption on the application state.

Workaround

If there is a reset in the RESETREAS register, ignore the wakeup reason.

3.23 [49] RADIO: First bits of on-air packet are not correct

This anomaly applies to Revision 1, build codes QFAA-A00.

Symptoms

First bits of the PAYLOAD field in the RADIO on-air packet are not correct.

Conditions

PCNF0.S1LEN is 4 or less and PCNF0.S1INCL is 1. RADIO is transmitting using 1 Mbps, 2 Mbps, or 4 Mbps data rate. The MCU power domain is powered down.

Consequences

Transmission is incorrect.

Workaround

Apply the following workaround:

```
*(volatile uint32_t *) 0x5008C58C = 1;
```

Alternatively, use Constant Latency sub-power mode before starting the radio.