nRF54L15 | nRF54L10 | nRF54L05
Preliminary Datasheet

NORDIC SEMICONDUCTOR

Contents

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nRF54L15, nRF54L10, and nRF54L05 make up the nRF54L Series. All wireless System-on-Chip (SoC) options in the series integrate an ultra-low power multiprotocol 2.4 GHz radio and MCU (Microcontroller Unit) functionality featuring a 128 MHz Arm® Cortex-M33 processor, comprehensive peripheral set, and scalable memory configurations up to 1524 KB NVM and up to 256 KB RAM.

Ultra-low power consumption is enabled with Nordic proprietary technologies such as low-leakage RAM and design expertise utilized in the advanced multiprotocol radio. With lower power consumption, each wireless SoC in the nRF54L Series enables improved battery lifetimes or reduced battery size.

Designed with versatility in mind, the nRF54L Series SoCs are suited to enable a broad range of applications. The multiprotocol 2.4 GHz radio supports the latest Bluetooth® 6.0 features including Bluetooth Channel Sounding, as well as 802.15.4-2020 for standards such as Thread®, Matter, and Zigbee®, and a proprietary 2.4 GHz mode supporting up to 4 Mbps for higher throughput. The devices integrate the peripherals expected in a wireless microcontroller enabling many products to be implemented with a single chip. An integrated RISC-V coprocessor further reduces the need for external ICs.

nRF54L Series wireless SoCs are available in a range of memory and package configurations, including pin-to-pin compatible options. With several memory options, finding the right device to fit an application optimizes cost and flexibility in design.

Key features

- 128 MHz Arm Cortex®-M33 processor
- Scalable memory configurations up to 1524 KB NVM and up to 256 KB RAM
- Multiprotocol 2.4 GHz radio supporting Bluetooth Low Energy, 802.15.4-2020, and 2.4 GHz proprietary modes (up to 4 Mbps)
- Comprehensive set of peripherals including new Global RTC available in System OFF, 14-bit ADC, and high-speed serial interfaces
- 128 MHz RISC-V coprocessor
- Advanced security including TrustZone® isolation, tamper detection and cryptographic engine side-channel leakage protection
- Ultra-compact packages
  - WLCSP 2.4x2.2 mm
  - QFN 6.0x6.0 mm

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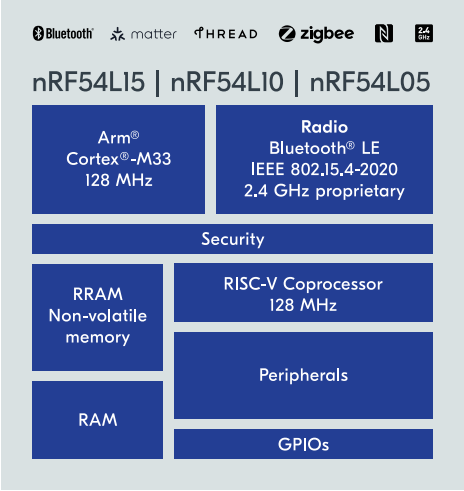

Power consumption highlights

Power mode	Current @ 3.0V
Active with radio	
Bluetooth LE TX 1 Mbps at 0 dBm	5.0 mA
Bluetooth LE TX 1 Mbps at +4 dBm	6.8 mA
Bluetooth LE RX 1 Mbps at +8 dBm	10.0 mA
Bluetooth LE RX 1 Mbps	3.2 mA
Active	
CPU CoreMark from RRAM with cache	2.4 mA
Sleep	
System ON IDLE with GRTC (XOSC) and 256 KB RAM	3.1 µA
System ON IDLE with GRTC (XOSC) and 192 KB RAM	2.6 µA
System ON IDLE with GRTC (XOSC) and 96 KB RAM	2.0 µA
System OFF with GRTC wakeup	0.8 µA
System OFF	0.6 uA

Product variants

Part number	NVM	RAM
nRF54L15	1524 KB	256 KB
nRF54L10	1012 KB	192 KB
nRF54L05	500 KB	96 KB

Features

Multiprotocol radio

- Bluetooth 6.0, IEEE 802.15.4-2020, and 2.4 GHz enabled transceiver
  - -96 dBm sensitivity in 1 Mbps Bluetooth Low Energy mode, 0.1% bit error rate
  - -104 dBm sensitivity in 125 kbps Bluetooth Low Energy mode (long range) with a 0.1% bit error rate
  - -102 dBm typical sensitivity in IEEE 802.15.4
  - Up to +8 dBm configurable output power; 1 dB step size from -8 dBm to +8 dBm
  - Supported data rates:
    - Bluetooth 6.0 – 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
    - IEEE 802.15.4-2020 – 250 kbps
    - Proprietary 2.4 GHz – 4 Mbps, 2 Mbps, and 1 Mbps
  - Single-ended antenna output (on-chip balun)
  - 128-bit AES/ECB/CCM/AAR coprocessor (on-the-fly operation)

Arm Cortex-M33 with TrustZone technology, 128 MHz

- 500 EEMBC CoreMark® score running from non-volatile memory, 3.90 CoreMark per MHz
- Single-precision floating-point unit (FPU)
- Memory protection unit (MPU)
- Digital signal processing (DSP) instructions
- Data watchpoint and trace (DWT), embedded trace macrocell (ETM), instrumentation trace macrocell (ITM), and cross trigger interface (CTI)
- Serial wire debug (SWD)
- Trace port interface unit (TPIU)
  - 4-bit parallel trace of ITM and ETM trace data
  - Serial wire output (SWO) trace of ITM data

Peripherals

- RISC-V Coprocessor
- Global RTC (GRTC) that can run in System OFF mode and implement a shared system timer
- Seven 32-bit timers with counter mode

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Features	

• RSSI (1 dB resolution)
 	
Platform security
 	
• Secure/non-secure memory protection
• Symmetric and asymmetric key crypto accelerator
• Secure key management
• Tamper detection
• Immutable boot partition
• Debug access port protection
• Individual watchdog timers for secure and non-secure context
 	
Memory
 	
• nRF54L15 – 1524 KB non-volatile memory (RRAM) and 256 KB RAM
• nRF54L10 – 1012 KB non-volatile memory (RRAM) and 192 KB RAM
• nRF54L05 – 500 KB non-volatile memory (RRAM) and 96 KB RAM
 	
Operating values
 	
• 1.7 V to 3.5 V supply and I/O voltage
• Single 32 MHz crystal operation
• Optional 32.768 kHz clock
• Operating temperature from -40°C to 105°C
	• Up to five fully featured serial interfaces with EasyDMA, supporting I^2C, SPI controller/peripheral, and UART
	  • One high-speed SPIM up to 32 MHz, four up to 8 MHz
	  • One high-speed UARTE up to 4 Mbps, four up to 1 Mbps
	  • I^2C up to 400 kHz
	• Three pulse width modulator (PWM) units with EasyDMA
	• I^2S two channel Inter-IC sound interface
	• ADC with up to eight programmable gain channels. 14-bit at 31.25 ksps, 12-bit at 250 ksps, and up to 10-bit at 2 Msps.
	• Pulse density modulation (PDM) interface
	• Near field communication (NFC)
	• Up to two quadrature decoders (QDEC)
	• Comparator and low-power comparator with wake-up from System OFF mode
	• Temperature sensor
	
	Package variants
	
	• QFN48 6.0x6.0 mm with 31 GPIO pins
	• WLCSP 2.4x2.2 mm with 32 GPIO pins
	  • 300 µm pitch

Revision history

About this document This document is organized into chapters that are based on the modules and peripherals available in the IC.

Product overview This document is applicable for the nRF54L15, nRF54L10, and nRF54L05 System-on-Chip devices. The main differences are memory, GPIO pin count, and package options, which are detailed in their respective sections.

Power and clock management The power and clock management system is optimized for ultra-low power applications to provide maximum power efficiency.

Event system The distributed programmable peripheral interconnect (DPPI) system enables peripherals to interact autonomously with each other through tasks and events, without intervention from the CPU.

Security The device is designed with state-of-the-art security features that include the following.

Peripherals The device features a rich set of peripherals. The following sections describe the peripherals and how they are used.

Debug and trace The debug and trace system is a flexible and powerful mechanism for non-intrusive debugging.

Recommended operating conditions The operating conditions are the physical parameters that the device can operate within.

Absolute maximum ratings Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the

reliability of the device.

Ordering information This chapter contains information on device marking, ordering codes, and container sizes.

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