PHY6236

Bluetooth Low Energy (BLE)/Private 2.4GHz System on Chip

Key Features

- 32-bit RISC-V MCU (Max 48MHz) with JTAG
- Memory
  - 8KB Retention SRAM
  - 8KB OTP
  - 80KB ROM
  - EEPROM (optional)
  - 128bit eFuse
- Up to 21 General Purpose I/O Pins
  - Configurable as serial interface and programmable IO MUX function mapping
  - All pins can be configured for wake-up
  - All pins for triggering interrupt
  - 6-channel PWM
  - 1-channel SPI Master
  - UART
  - USB 2.0
  - DMA
  - NRZ coded LED driver
- 10-channel 800KHz 12bit ADC
- Advanced control timer
  - 16-bit up, down, up/down auto-reload counter
  - 16-bit programmable prescaler allowing dividing the counter clock frequency either by any factor between 1 and 65536
  - Up to 4 independent channels for input capture, output compare, PWM generation and one-pulse mode output
- 1 Watchdog Timer
- Real Timer Counter (RTC)
- Power, Clock, Reset Controller
- Flexible Power management
  - Operating voltage range 1.8V to 5.5V
  - Embedded LDOs
  - Battery monitor: support low battery detection
- Power Consumption
  - 1uA@3V OFF mode (IO wake up only)
  - 2uA@3V sleep mode with 32KHz RTC
  - Receive Mode: 10mA@3.3V Power Supply
  - Transmit Mode: 10mA (0dBm output power) @3.3V Power Supply
- RC Oscillator Hardware Calibrations
  - 32KHz RC osc for RTC with +/-200ppm accuracy
  - 32MHz RC osc for HCLK with 3% accuracy
- BLE
  - Bluetooth SIG 5.4
  - Support Master & Slave
- 2.4 GHz Transceiver
  - Support BLE 5.4 RF PHY 1Mbps/2Mbps
  - Proprietary programmable 31.25kbps~1Mbps data rates
  - FSK with configurable Gaussian filter (configurable modulation index)
  - Sensitivity:
    -96dBm@BLE 1Mbps data rate
    -93dBm@BLE 2Mbps data rate
  - TX power -20 to +10dBm in 3dB steps
  - Single-pin antenna: no RF matching or RX/TX switching required
  - RSSI (1dB resolution)
- AES-128 Encryption Hardware
- Operating Temperature: -40˚C ~+105˚C
- RoHS Package: SSOP24/SOP16/SOP8

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Revision History

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1 Introduction

PHY6236 is a System on Chip (SoC) for Bluetooth® low energy and proprietary 2.4G applications. It has high-performance low-power 32-bit RISC-V MCU with 8KB retention SRAM, 80KB ROM, 8KB OTP, and an ultra-low power, high performance, multi-mode radio. Also, PHY6236 can support BLE with security and application. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

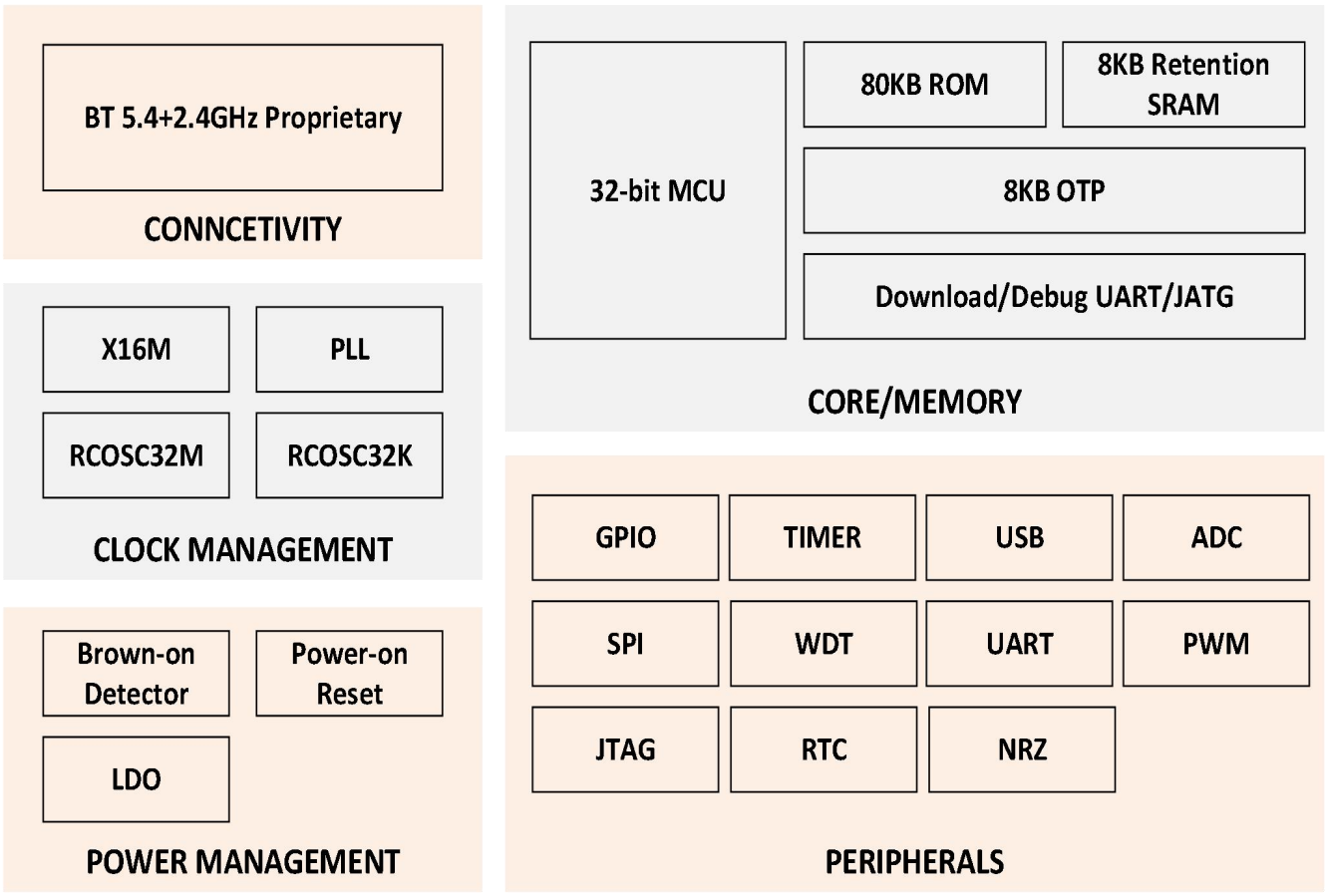


Figure 1: PHY6236 Block Diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the package types of SSOP24, SOP16 and SOP8.

2.2.1 PHY6236 (SSOP24)

2.2.1.1 Pin Assignment

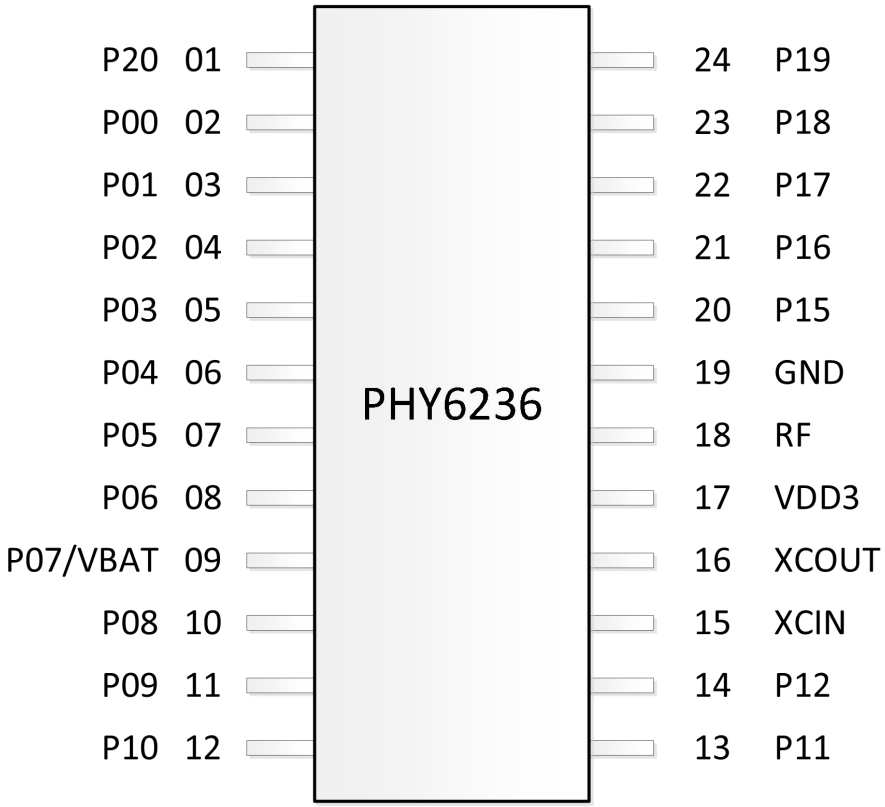


Figure 2: Pin assignment – PHY6236 SSOP24 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	P20	GPIO 20/Full mux
2	P0	GPIO 00/Full mux
3	P01	GPIO 01/Full mux
4	P02	GPIO 02/Full mux
5	P03	GPIO 03/Full mux
6	P04	GPIO 04/Full mux
7	P05	GPIO 05/Full mux
8	P06	GPIO 06/Full mux
9	P07/VBAT	GPIO 07/Full mux/VBAT
10	P08	GPIO 08/Full mux
11	P09	GPIO 09/Full mux
12	P10	GPIO 10/Full mux

Pin	Pin name	Description
13	P11	GPIO 11/Full mux
14	P12	GPIO 12/Full mux
15	XCIN	16MHz crystal input
16	XCOUT	16MHz crystal output
17	VDD3	3.3V power supply
18	RF	RF antenna
19	GND	GND
20	P15	GPIO 15/Full mux
21	P16	GPIO 16/Full mux
22	P17	GPIO 17/Full mux
23	P18	GPIO 18/Full mux
24	P19	GPIO 19/Full mux

Table 1: Pin functions of PHY6236 SSOP24 package

2.2.2 PHY6236 (SOP16)

2.2.2.1 Pin Assignment

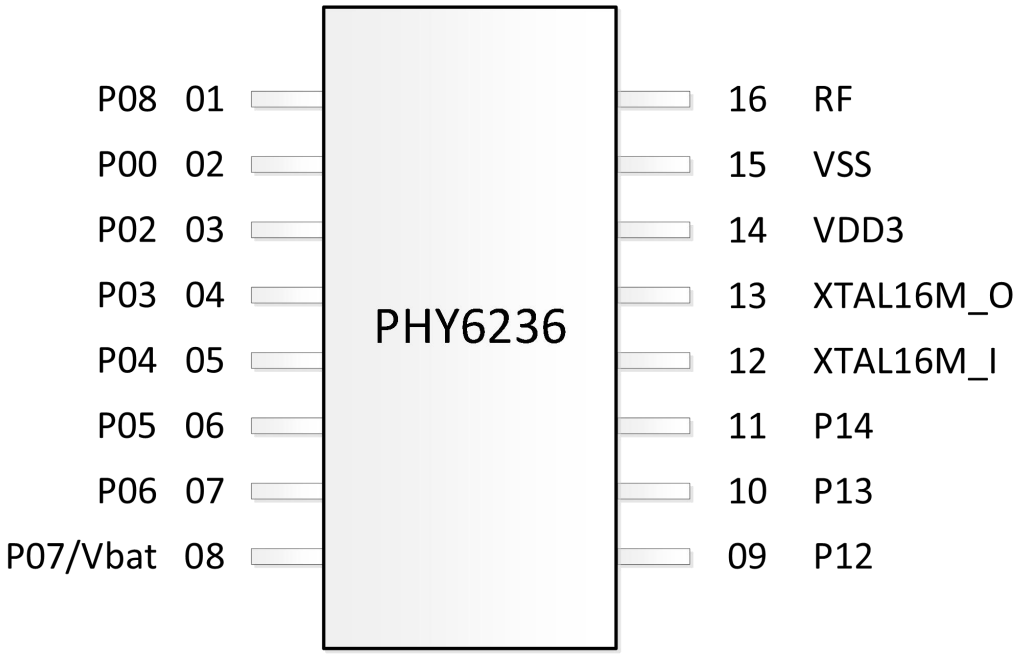


Figure 3: Pin assignment – PHY6236 SOP16 package

2.2.2.2 Pin Functions

Pin	Pin name	Description
1	P08	GPIO 08/Full mux
2	P00	GPIO 00/Full mux
3	P02	GPIO 02/Full mux
4	P03	GPIO 03/Full mux
5	P04	GPIO 04/Full mux
6	P05	GPIO 05/Full mux

7	P06	GPIO 06/Full mux
8	P07/Vbat	GPIO 07/Full mux
9	P12	GPIO 12/Full mux
10	P13	GPIO 13/Full mux
11	P14	GPIO 14/Full mux
12	xtal_in	16MHz crystal input
13	xtal_out	16MHz crystal output
14	VDD3	3.3V power supply
15	VSS	GND
16	RF	RF antenna

Table 2: Pin functions of PHY6236 SOP16 package

2.2.3 PHY6236 (SOP8)

2.2.3.1 Pin Assignment

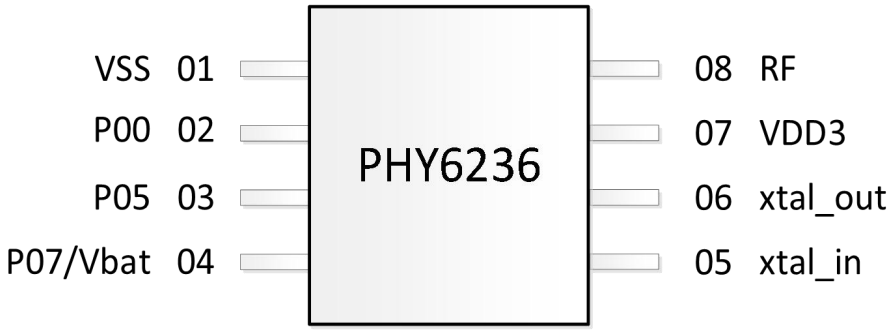


Figure 4: Pin assignment – PHY6236 SOP8 package

2.2.3.2 Pin Functions

Pin	Pin name	Description
1	VSS	GND
2	P00	GPIO 00/Full mux
3	P05	GPIO 05/Full mux
4	P07/Vbat	GPIO 07/Vbat/Full mux
5	xtal_in	16MHz crystal input
6	xtal_out	16MHz crystal output
7	VDD3	3.3V power supply
8	RF	RF antenna

Table 3: Pin functions of PHY6236 SOP8 package

3 System Block

The system block diagram of PHY6236 is shown in **Figure 1**.

3.1 Memory

PHY6236 has total 80KB ROM, 8KB SRAM and 8KB OTP. The physical address space of these memories is shown in **Figure 5**.

FEMTO Memory Space

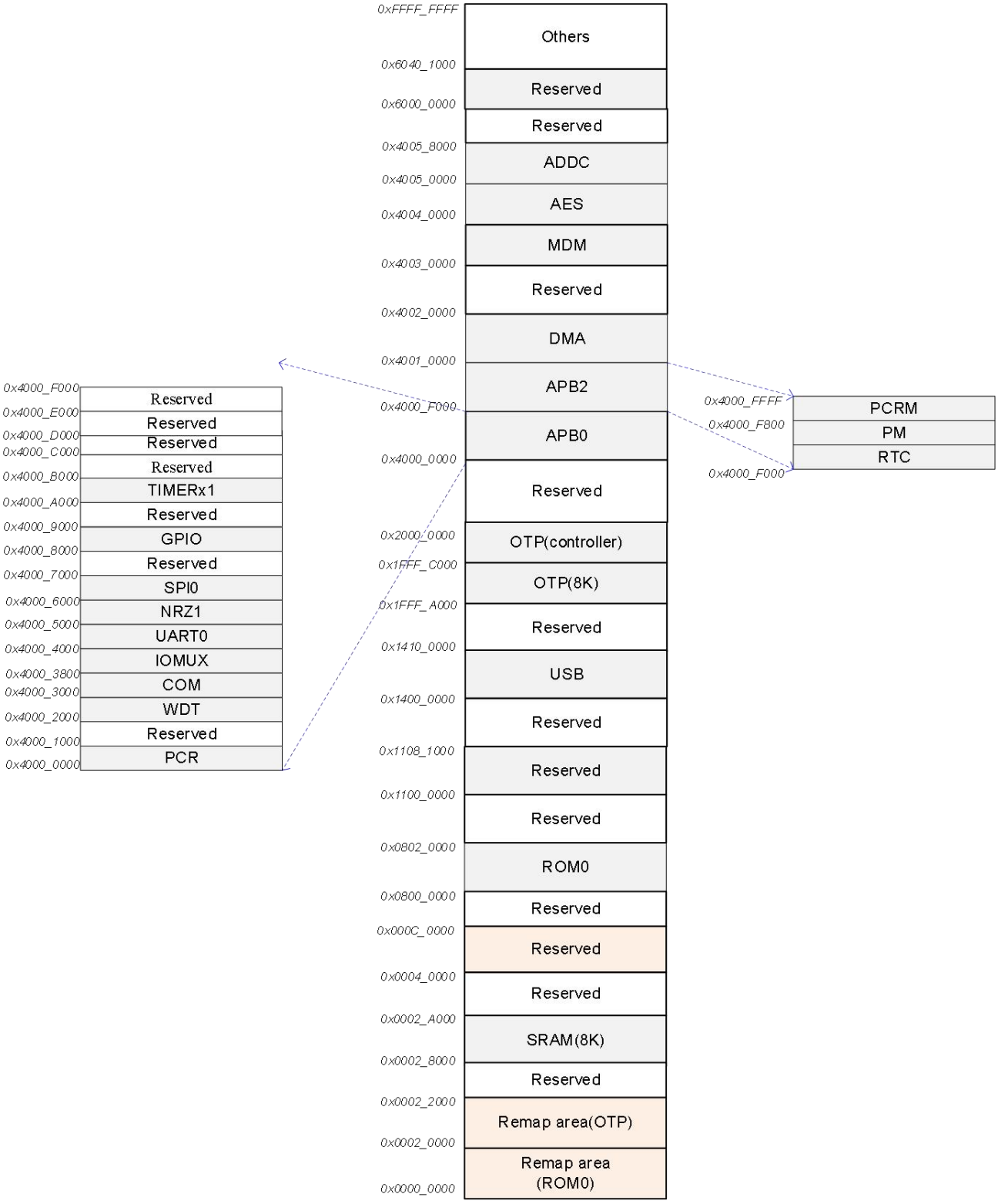


Figure 5: PHY6236 Memory Space

3.2 CPU

The PHY6236 has a high-performance low-power 32-bit CPU(N205). The CPU, memories, and all peripherals are connected by AMBA bus fabrics.

The CPU will play controller role in BLE modem and run all user applications.

The N205 have the following features:

• CPU Core

– 2-pipeline stages , using state-of-the-art processor micro-architecture to deliver the best-of-class performance efficiency and lowest cost.

– dynamic branch predictor.

– instruction prefetch logic, which can prefetch subsequent two instructions to hide the instruction memory access latency.

• Support Instruction Set Architecture (ISA)

– The N205 is a 32-bit RISC-V Processor Core, supporting the combination of RV32I/E/M/A/C/B instruction extensions.

– Misaligned memory access hardware support (Load/Store instructions).

• Support Bit-Manipulation ISA Extensions

– Zba: Address generation instructions.

– Zbb: Basic bit-manipulation.

– Zbc: Carry-less multiplication.

– Zbs: Single-bit instructions.

• Bus Interfaces

– Support 32-bit wide standard AHB-Lite system bus interface for accessing system instruction and data.

– Support 32-bit wide Instruction Local Memory (ILM) bus interface for accessing private instruction local memory.

– Support 32-bit wide Data Local Memory (DLM) bus interface for accessing private data local memory.

– Support 32-bit wide Slave Port (SLAVE) bus interface (with standard AHB-Lite interface protocol) for external device (DMA or other masters) to access internal ILM/DLM.

• Low-Power Management

– Support WFI (Wait For Interrupt) and WFE (Wait For Event) scheme to enter sleep mode.

– Support two-level sleep modes: shallow sleep mode, and deep sleep mode.

• Core-Private Timer Unit (TIMER)

– 64-bits wide real-time counter.

– Support the generation of the timer interrupt defined by the RISC-V standard.

– Support the generation of the precise periodic timer interrupt (can be used as System Tick) with auto clear-to-zero mode.

– Support the generation of software interrupt defined by the RISC-V standard.

• Enhanced Core Level Interrupt Controller (ECLIC)

– Support the RISC-V architecturally defined software, timer and external interrupts.

– Support configurable number of interrupt levels and priorities, and support software dynamically programmable division of interrupt levels and priorities values.

– Support interrupts preemption based on interrupt levels.

– Support vectored interrupt processing mode for extremely fast interrupt response (6 cycles).

– Support fast interrupts tail-chaining mechanism.

• Memory Protection

– Support configurable Physical Memory Protection (PMP) to protect the memory

3.2.1 ROM

PHY6236 has 1 ROM.

	SIZE	CONTENT
ROM	80KB	Boot ROM. Protocol stack. Common peripheral drivers. ATE AT command.

Table 4: List of ROM

3.2.2 SRAM

PHY6236 has 1 SRAM blocks. The SRAM block have retention capability, which can be configured individually. Normal operating voltage is 1.2V, and the voltage is adjustable at retention. The SRAM block can be used to store program or data.

	SIZE	CONTENT
SRAM0	8KB	

Table 5: List of SRAM

3.2.3 OTP

The OTP is an antifuse based technology, which is capable for security code storage. When writing data to this IP, a voltage of 6.5V needs to be applied. The main memory is organized as 2048 by 32 bits. The OTP cell design will provide a low cost logic process OTP approach compared with alternative approaches. The OTP is programmed by 1.2V, 3.3V power supply.

3.2.4 eFuse

PHY6236 integrates 128bits internal nonvolatile one-time programmable EFUSE storage. With a 8-bit

parallel interface, 1-bit can be programmed at one clock in program mode and 8-bit can be read at one time in read mode.

3.2.5 Memory Address Mapping

Name	Size	Master	Physical Address
ROM	80K	MCU	0800_0000~0801_FFFF
SRAM	8K	MCU/DMA	0002_8000~0002_9FFF
OTP	8K	MCU/DMA	1FFF_A000~1FFF_BFFF

Table 6: Memory address mapping

3.3 Boot and Execution Modes

Only in CP Chip form, the chip enters CP boot mode after power on. ROM1 is then aliased to the 0x0 address and the chip program starts from ROM1.

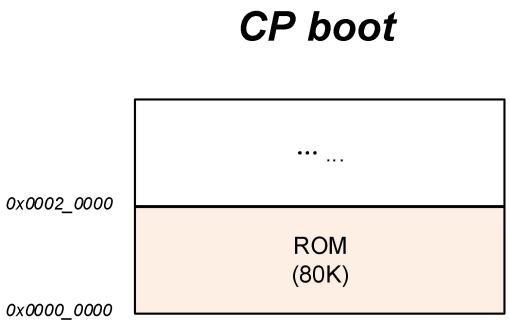


Figure 6: PHY6236 boot mode

3.4 Power, Clock and Reset (PCR)

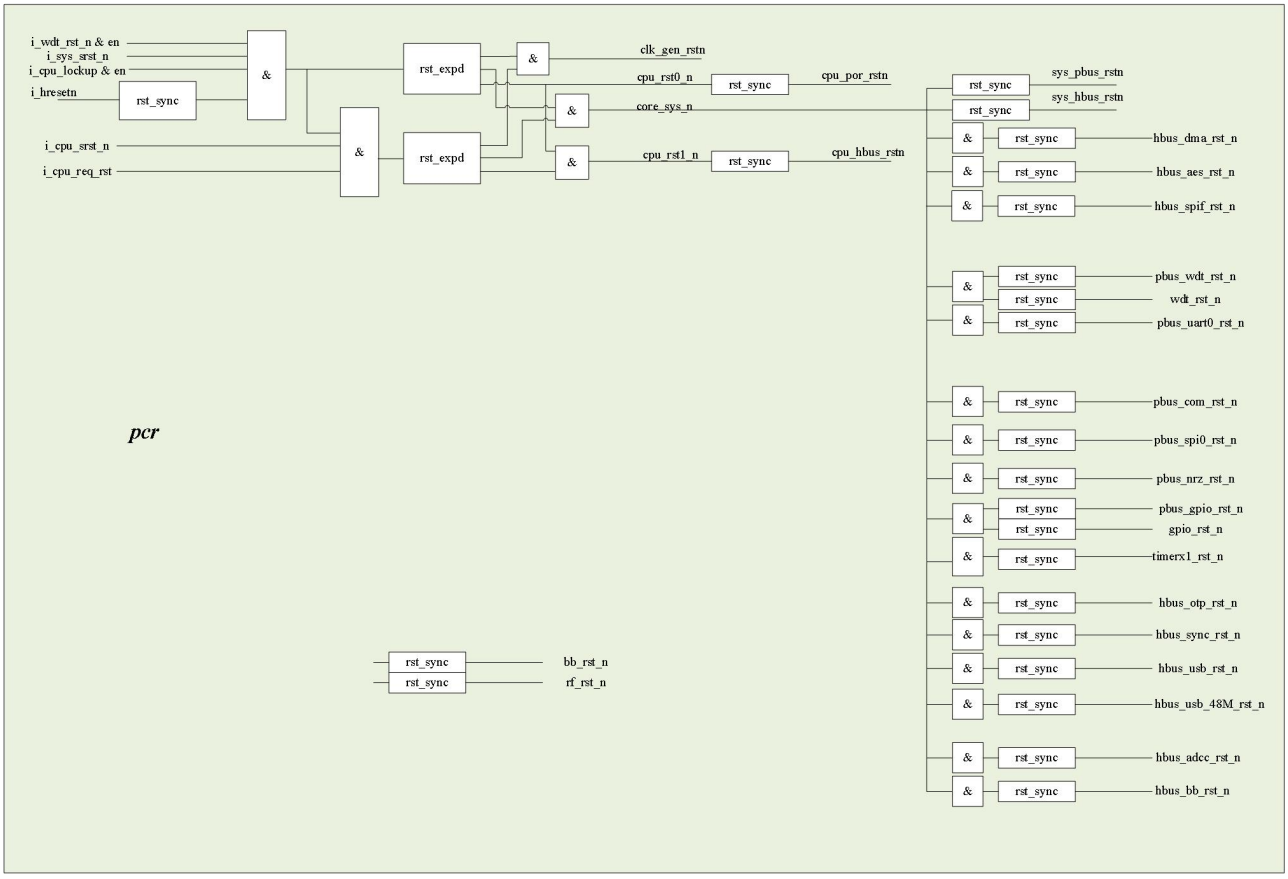


Figure 7: PHY6236 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on

depending on needed application functionality.

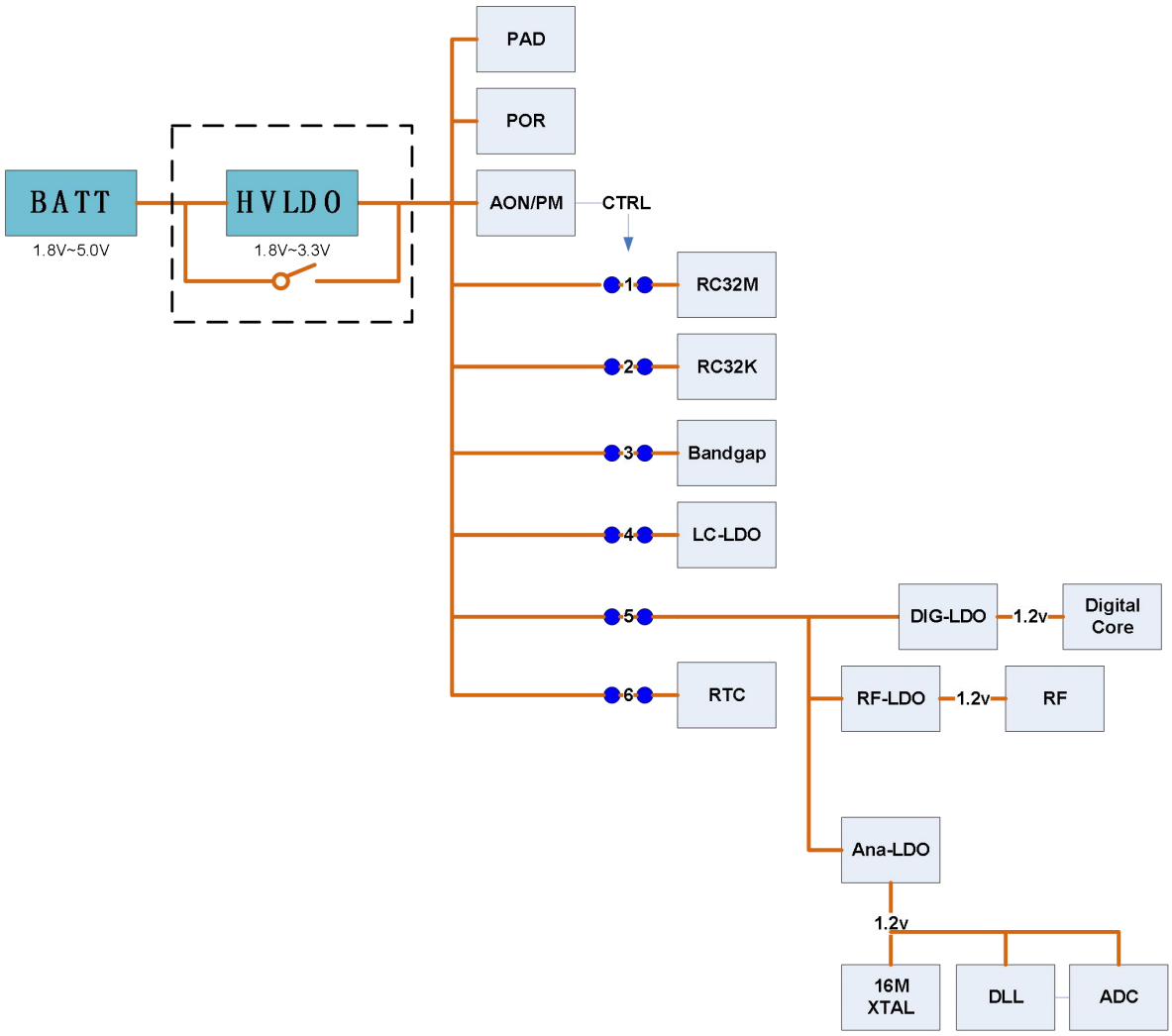


Figure 8: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

#	Switch	Normal	Sleep	Off
1	RC32M	On	Off	Off
2	RC32K	On	Optional	Off
3	bandgap	On	Off	Off
4	LC-LDO	On	on	Off
5	DIG-LDO	On	Off	Off
6	RTC	On	Optional	Off

Table 7: Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include:

- IOs
- RESET
- UVLO reset

3.6.1.5 UVLO

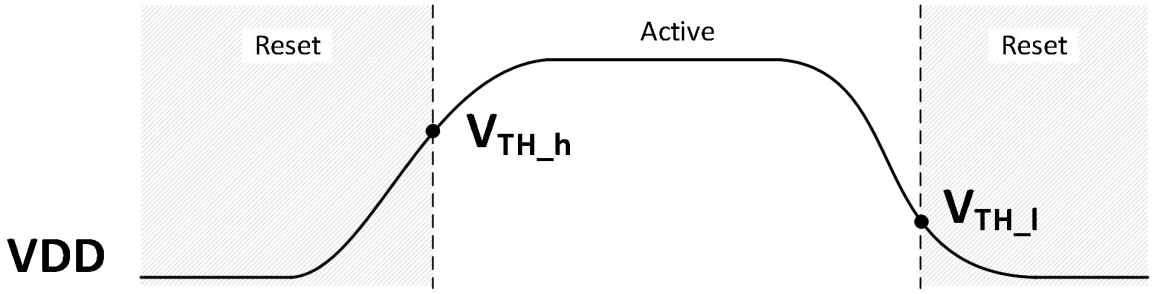


Figure 9: UVLO reset

VDD > VTH_h, release reset; VDD < VTH_l, enter reset.

VDD	Min.	TYP	Max.	Unit
V_{TH_h}	1.7	1.74	1.78	V
V_{TH_l}	1.63	1.66	1.69	V

Table 8: UVLO

If power supply VDD rises more than 0.6V within 100us, power monitor will trigger a whole chip reset event.

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	MCU Interrupt Number
	0
xtal_irq	1
	2
r2_bb_sch_irq	3
r2_bb_irq	4
	5
	6
efuse_irq	7
	8
	9
wdt_irq	10
uart0_irq	11
	12
spif_protect_irq	13
	14
spi0_irq	15
gpio_irq	16
	17
	18
dma_int	19
	20
nrz1_irq	21
	22
	23
timerx_irq	24
	25
	26
otgtop_int	27
	28
adcc_irq	29
	30
hclk_mux_done	31

Table 9: Interrupts

3.8 Clock Management

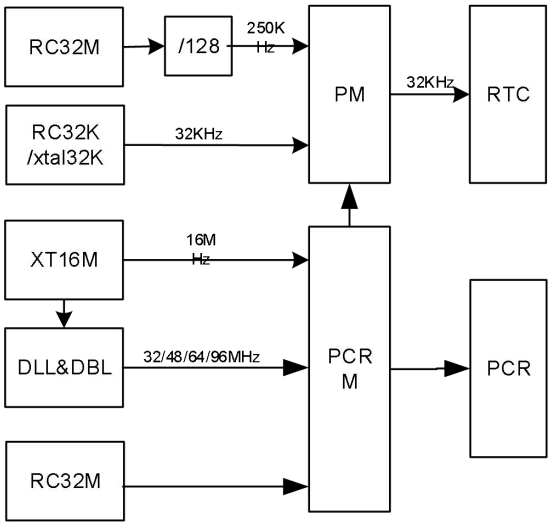


Figure 10: Clock management

There is only one crystal clock sources: 16MHz crystal oscillator (XT16M). There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48MHz.

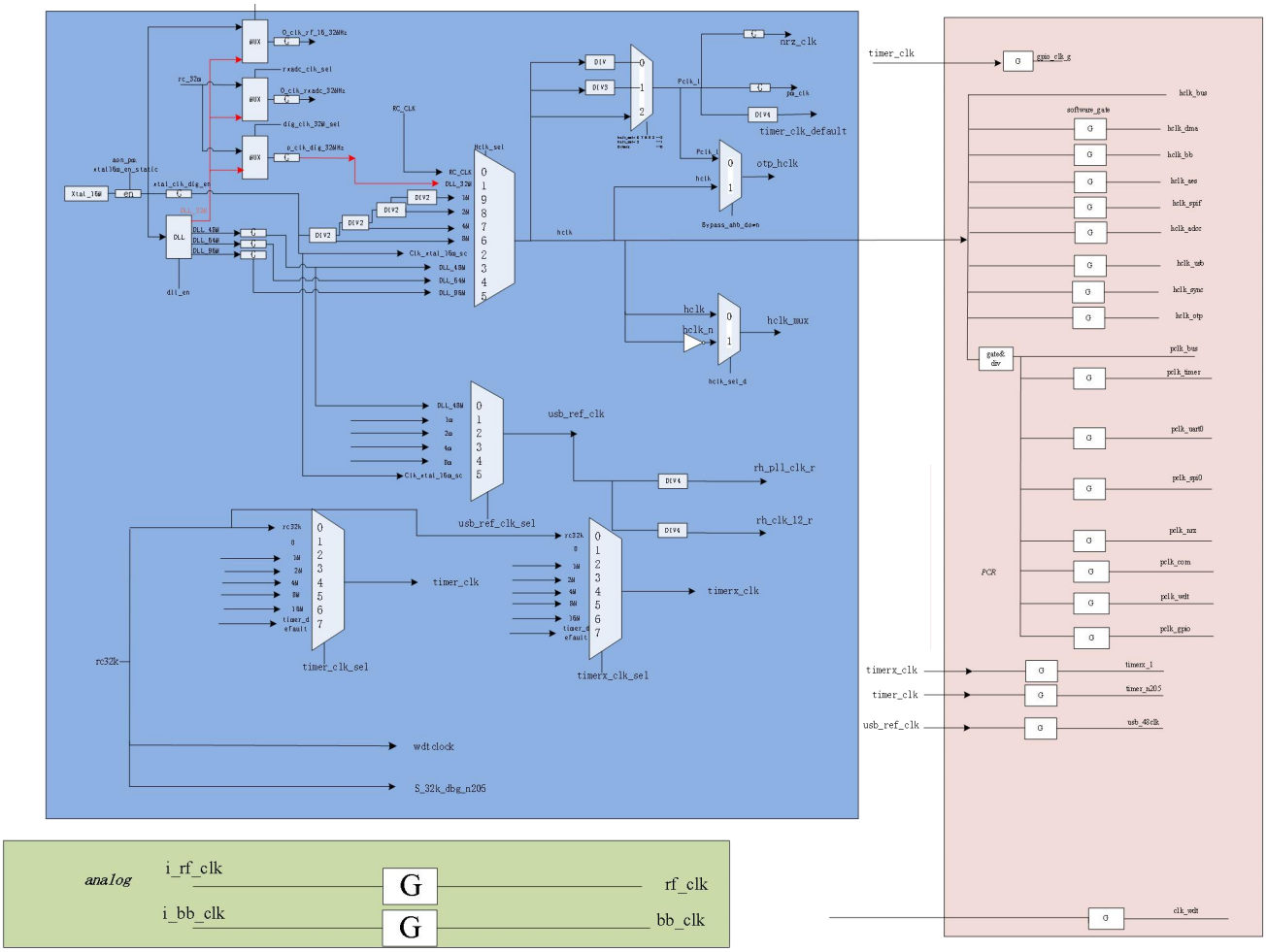


Figure 11: Clock Structure Diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to specific physical I/O pads (I/O at die boundary). These peripheral modules include I2C, UART, USB, PWM 0-5, SPI, etc. However, for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include JTAG, analog_ios and GPIOs.

Figure 12 below shows the IOMUX functional diagram.

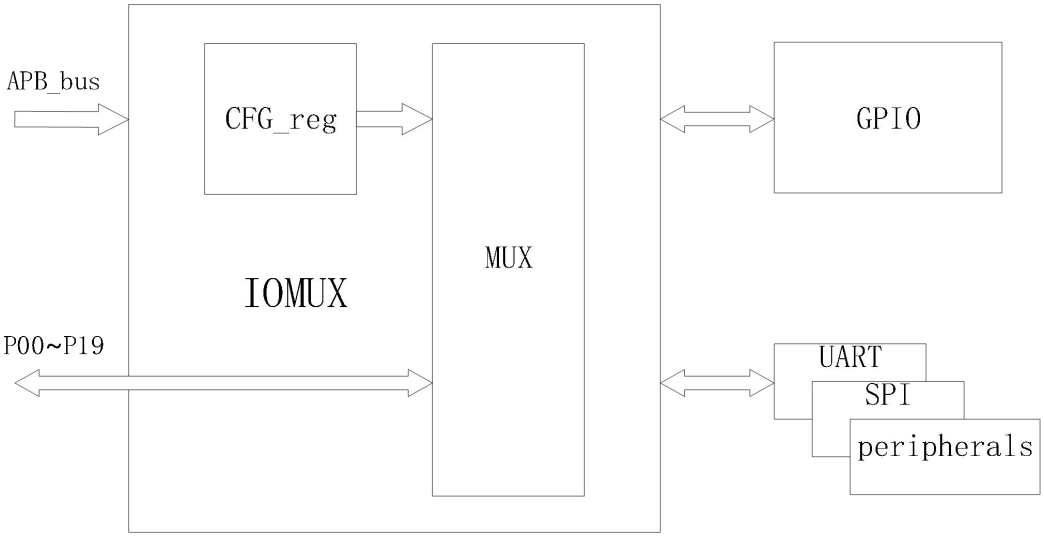


Figure 12: IOMUX structure diagram

There are 21 configurable pads. The table blow shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C, UART, PWM 0-5 and SPI.

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: analog I/Os (ADC inputs) and GPIO. When they are enabled, their IOs are mapped to physical pads according to the following table.

#	PHY6236	Normal Mode (p8=0@reset active)	
0	GPIO_P00	GPIO	
1	GPIO_P01	GPIO	
2	GPIO_P02	JTAG_TMS_IO	
3	GPIO_P03	JTAG_TCK	
4	GPIO_P04	GPIO	analog_io[0]/adc_ch[1]
5	GPIO_P05	GPIO	analog_io[1]/adc_ch[7]
6	GPIO_P06	GPIO	analog_io[2]/adc_ch[2]
7	GPIO_P07	GPIO	
8	GPIO_P08	GPIO	
9	GPIO_P09	GPIO	analog_io[3]/adc_ch[8]
10	GPIO_P10	GPIO	analog_io[4]/adc_ch[3]
11	GPIO_P11	GPIO	analog_io[5]/adc_ch[9]
12	GPIO_P12	GPIO	analog_io[6]/adc_ch[4]
13	GPIO_P13	GPIO	analog_io[7]/adc_ch[10]
14	GPIO_P14	GPIO	analog_io[8]/adc_ch[5]
15	GPIO_P15	GPIO	analog_io[9]/adc_ch[11]
16	GPIO_P16	GPIO	
17	GPIO_P17	GPIO	
18	GPIO_P18	GPIO	
19	GPIO_P19	GPIO	
20	GPIO_P20	GPIO	

Table 10: Peripheral IO mapped through IOMUX (special purpose)

In the IOMUX table above, the first column is the IO pad mapping in default mode, when no IOMUX function is selected and no special purpose peripherals such as analog IO, GPIO<0:3>, are enabled. In this mode, pin<2:3> are used for CJTAG.
When analog IOs are enabled, pins<4:6>, <9:15> are connected to internal analog IOs. More specifically, analog_io<0:9> are connected to ADC inputs.

In JTAG mode, data output for JTAG test mode is mapped to P00; data input for JTAG test mode is mapped to P01; mode control input for JTAG test mode is mapped to P02; clock input for JTAG test mode is mapped to P03.

3.10 GPIO

The General Purpose I/Os are a type of peripheral that can be mapped to physical I/O pads and programmed by software. The flexible GPIO are organized as PORT A. PortA has bi-direction 20 bit lines, e.g., GPIO_PORT A [20:0]. With default setting, physical pads: P00-P20 are connected to PortA. When all GPIOs are enabled, as described in the IOMUX table in IOMUX section.

All PortA pins can be configured as bi-directional serial interface, by selecting as input or output direction, and their corresponding data can be either read from or written to registers. All PortA and pins support wake-up and debounce function, and all pins support interrupt.

Each GPIO pins can be pulled up to VDD3 or pulled down to ground by adding pull up or pull down resistors to have default functions/states.

For more detailed info, please refer to “PHY623x GPIO Application Notes”, in software SDK document folder.

#	PHY6236	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
0	GPIO_P00 / VPP	GPIO	IN	√	√	
1	GPIO_P01	GPIO	IN	√	√	
2	GPIO_P02	JTAG_TMS_IO	OUT	√	√	
3	GPIO_P03	JTAG_TCK	IN	√	√	
4	GPIO_P04	GPIO	IN	√	√	io_aio[0]
5	GPIO_P05	GPIO	IN	√	√	io_aio[1]
6	GPIO_P06	GPIO	IN	√	√	io_aio[2]
7	GPIO_P07	GPIO	IN	√	√	
8	GPIO_P08	GPIO	IN	√	√	
9	GPIO_P09	GPIO	IN	√	√	io_aio[3]
10	GPIO_P10	GPIO	IN	√	√	io_aio[4]
11	GPIO_P11	GPIO	IN	√	√	io_aio[5]
12	GPIO_P12	GPIO	IN	√	√	io_aio[6]
13	GPIO_P13	GPIO	IN	√	√	io_aio[7]
14	GPIO_P14	GPIO	IN	√	√	io_aio[8]
15	GPIO_P15	GPIO	IN	√	√	io_aio[9]
16	GPIO_P16	GPIO	IN	√	√	
17	GPIO_P17	GPIO	IN	√	√	
18	GPIO_P18	GPIO	IN	√	√	
19	GPIO_P19	GPIO	IN	√	√	
20	GPIO_P20	GPIO	IN	√	√	

Table 11: PHY6236 GPIO Application Notes

3.10.1 DC Characteristics

TA=25℃, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 12: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*® low energy (BLE) protocol implementations.

- General modulation format
- FSK (configurable modulation index) with configurable Gaussian Filter Shaping
- On-air data rates
- 1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
- -96dBm@1Mbps BLE
- -93dBm@2Mbps BLE
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Advanced control timer

The advanced-control timers consist of a 16-bit auto-reload counter driven by a programmable prescaler. Timer features include:

- 16-bit up, down, up/down auto-reload counter.
- 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536.
- Up to 4 independent channels for:
  - – Input capture
  - – Output compare
  - – PWM generation (Edge and Center-aligned Mode)
  - – One-pulse mode output
- Complementary outputs with programmable dead-time.
- Synchronization circuit to control the timer with external signals and to interconnect several timers together.
- Repetition counter to update the timer registers only after a given number of cycles of the counter.
- Break input to put the timer’s output signals in reset state or in a known state.
- Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes.

- Trigger input for external clock or cycle-by-cycle current management.
- Interrupt/DMA generation on the following events:

  – Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)

  – Trigger event (counter start, stop, initialization or count by internal/external trigger)

  – Input capture

  – Output compare

  – Break input

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24-bit COUNTER, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128-bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.6 SPI

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. The SPI is master only.

4.7 UART

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

4.8 Pulse Width Modulation (PWM)

PHY6236 supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual

counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

Duty_cycle_PWM = N_threshold/N_top_count;

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following **Figure 13**, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers 0x4000_E000<0><4> to allow all PWM channels can be programmed. For details please refer to documents of PHY623x register tables.

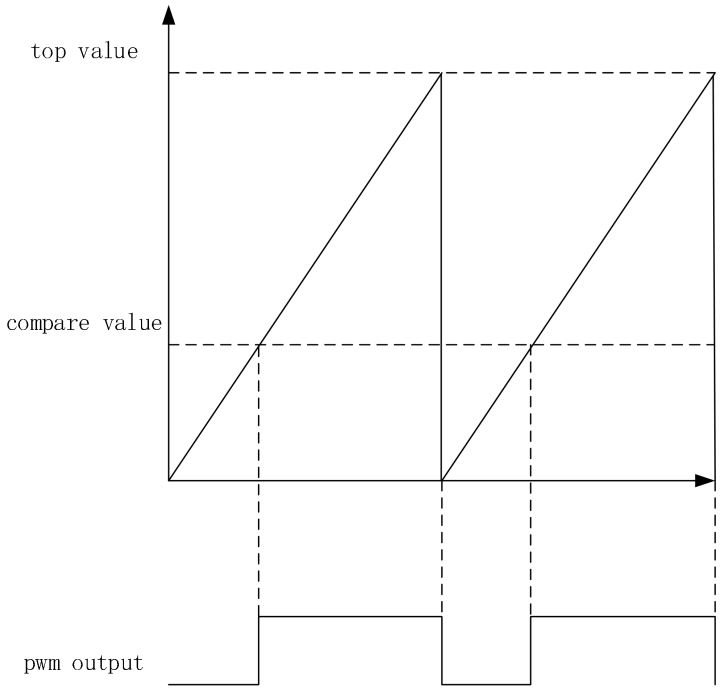


Figure 13: PWM operation

4.9 USB Controller

The USB controller is compatible with the full speed(FS) and low speed(LS) USB specification. It provides 5 endpoints: EP0 IN/OUT supports input and output control data transfer;EP1~EP3 IN support input interrupt data transfer; EP4 OUT support output interrupt data transfer.

4.10 Analog to Digital Converter (ADC)

The 12bit SAR ADC has total 12 inputs. Among them, there are two for VDD3 and VBAT detection, and 10 channel for external IO input, which can be programmed to 5 pairs of differential input or 10 single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with max 800KHz ADC sampling rate.

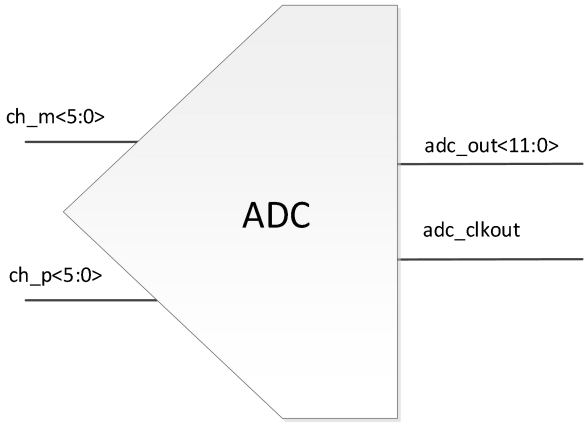


Figure 14: ADC

4.10.1 ADC Channel Connectivity

ADC	Hardwired	ADC_channel	differential	note
aio<0>	gpio<4>	Ch_sel: 1		
aio<1>	gpio<5>	Ch_sel: 7		
aio<2>	gpio<6>	Ch_sel: 2		
aio<3>	gpio<9>	Ch_sel: 8		
aio<4>	gpio<10>	Ch_sel: 3		
aio<5>	gpio<11>	Ch_sel: 8		
aio<6>	gpio<12>	Ch_sel: 4		
aio<7>	gpio<13>	Ch_sel: 10		
aio<8>	gpio<14>	Ch_sel: 5	-	
aio<9>	gpio<15>	Ch_sel: 11	-	
Vdd3/2	Vdd3/2	Ch_sel: 0		
Vbat/3	Vbat/3	Ch_sel: 6		

Table 13: ADC channel connectivity

Aio<9:7,4:0>can be selected through an analog Mux by programming aio_pass<7:0> and aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input B negative.

0x4000F8C4			i_analog_ctrl1	register description
[31:30]	RO	2'h0	reserved	

[19]	RW	1'h0	vbat_det_ctrl	enable sample vbat/3
[18]	RW	1'h0	vdd3_det_ctrl	enable sample vdd3/2
[17]	RW	18'h0	aio_det_ctrl_9	enable sample aio[9]/P15
[16]	RW	18'h0	aio_det_ctrl_8	enable sample aio[8]/P14
[15]	RW	18'h0	aio_det_ctrl_7	enable sample aio[7]/P13
[14]	RW	18'h0	aio_det_ctrl_6	enable sample aio[6]/P12
[13]	RW	18'h0	aio_det_ctrl_5	enable sample aio[5]/P11
[12]	RW	18'h0	aio_det_ctrl_4	enable sample aio[4]/P10
[11]	RW	18'h0	aio_det_ctrl_3	enable sample aio[3]/P9
[10]	RW	18'h0	aio_det_ctrl_2	enable sample aio[2]/P6
[9]	RW	18'h0	aio_det_ctrl_1	enable sample aio[1]/P5
[8]	RW	18'h0	aio_det_ctrl_0	enable sample aio[0]/P4
[7:4]	RO	4'h0	reserved	
[3:1]	RW	3'h0	~~reserved1~~	
[0]	RW	1'h0	~~reserved2~~	

Table 14: analog Mux

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which PHY6236 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the PHY6236. **Table 15** specifies the absolute maximum ratings for PHY6236.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
Vbus		-0.3	+5.5	V
Vbat		-0.3	+5.5	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+105	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDMQF	Charged Device Model (SSOP24, SOP16 and SOP8 package)		500	V

Table 15: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that PHY6236 can operate within as defined in **Table 16**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
Vbus	Supply voltage	4.5	5	5.5	V
Vbat	Supply voltage	3.0	3.7	5.5	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA	Operating temperature	-40	27	105	°C

Table 16: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	@3V		10		mA
Rx Only	@3V		10		mA

Table 17: Radio current consumption

7.2 Transmitter Specification

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 18: Transmitter specification

7.3 Receiver Specification

7.3.1 RX BLE 1Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-96		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB

Parameter	Description	MIN	TYP	MAX	UNIT
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 19: RX BLE 1Mbps GFSK

7.3.2 RX BLE 2Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-93		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 20: RX BLE 2Mbps GFSK

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 21: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 22: Glossary

9 Ordering information

9.1 Chip Marking Example

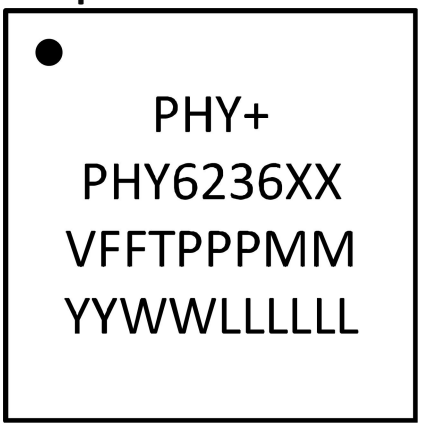


Figure 15: Chip Marking Example

9.2 Chip Marking Rule

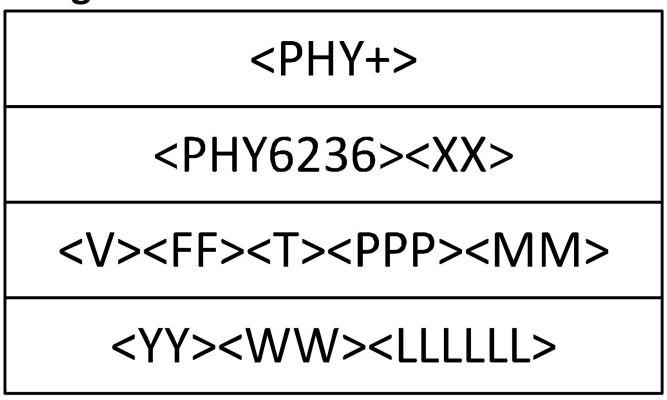


Figure 16: Chip Marking Rule

Abbreviation	Definition and Implemented Codes
<PHY+>	PHYPLUS MICROELECTRONIC
<PHY6236>	PHY6236 Product
<XX>	Package Type
<V>	Supply Voltage
<FF>	EEPROM Size
<T>	Operating Temperature
<PPP>	Product Information
<MM>	Manufacturer Information
<YY>	2-digital Year Code
<WW>	2-digital Week Code
<LLLLLL>	6-digital Wafer Lot Code

Table 23: Chip Marking Rule

9.3 Order Code

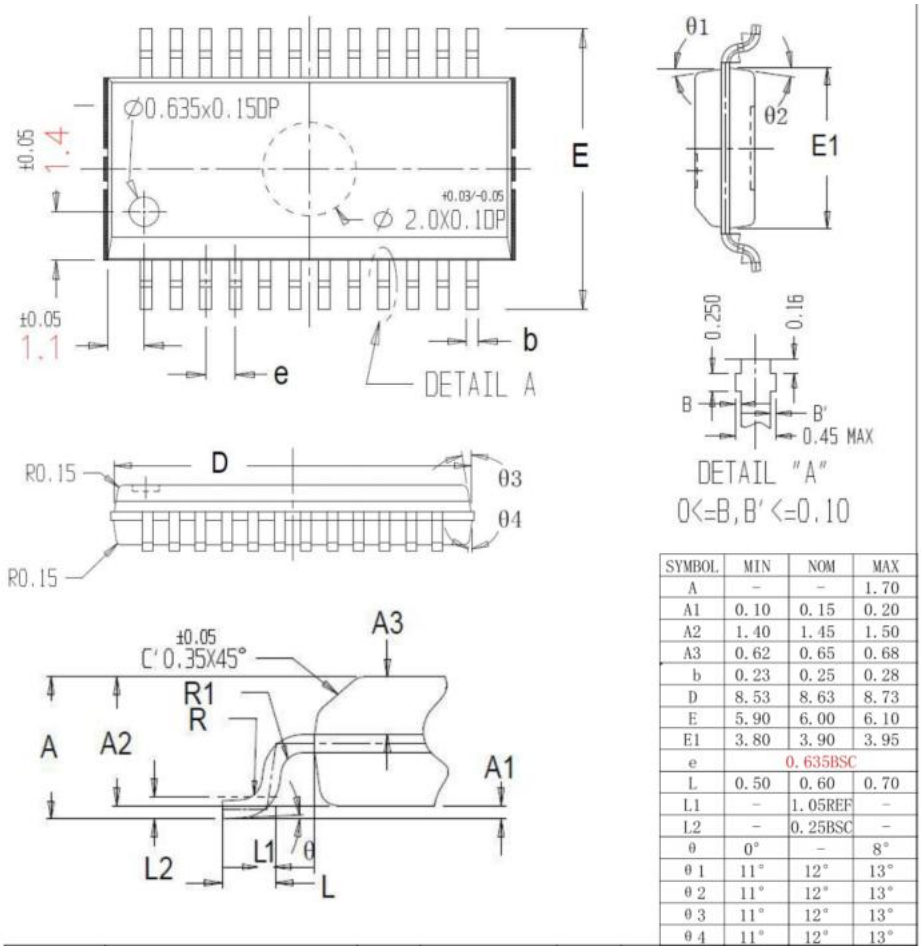
Part No.	Package	Supply Voltage	Operating Temp. (° C)	EEPROM	Packing	Quantity			
						ea /tube	tube /inner	inner /case	ea /case
PHY6236SC-W00C	SOP16	1.8~5.5V	-40~105	/	Tube	50	100	10	50000
PHY6236SD-W00C	SSOP24	1.8~5.5V	-40~105	/	Tube	50	100	10	50000
PHY6236SG-W00C	SOP8	1.8~5.5V	-40~105	/	Tube	50	100	10	50000
PHY6236SC-WE2I	SOP16	1.8~5.5V	-40~105	2kb	Tube	50	100	10	50000
PHY6236SD-WE2I	SSOP24	1.8~5.5V	-40~105	2kb	Tube	50	100	10	50000

Table 24: Order Code

10 Package Dimensions

Note: dimensions are in mm, angels are in degree.

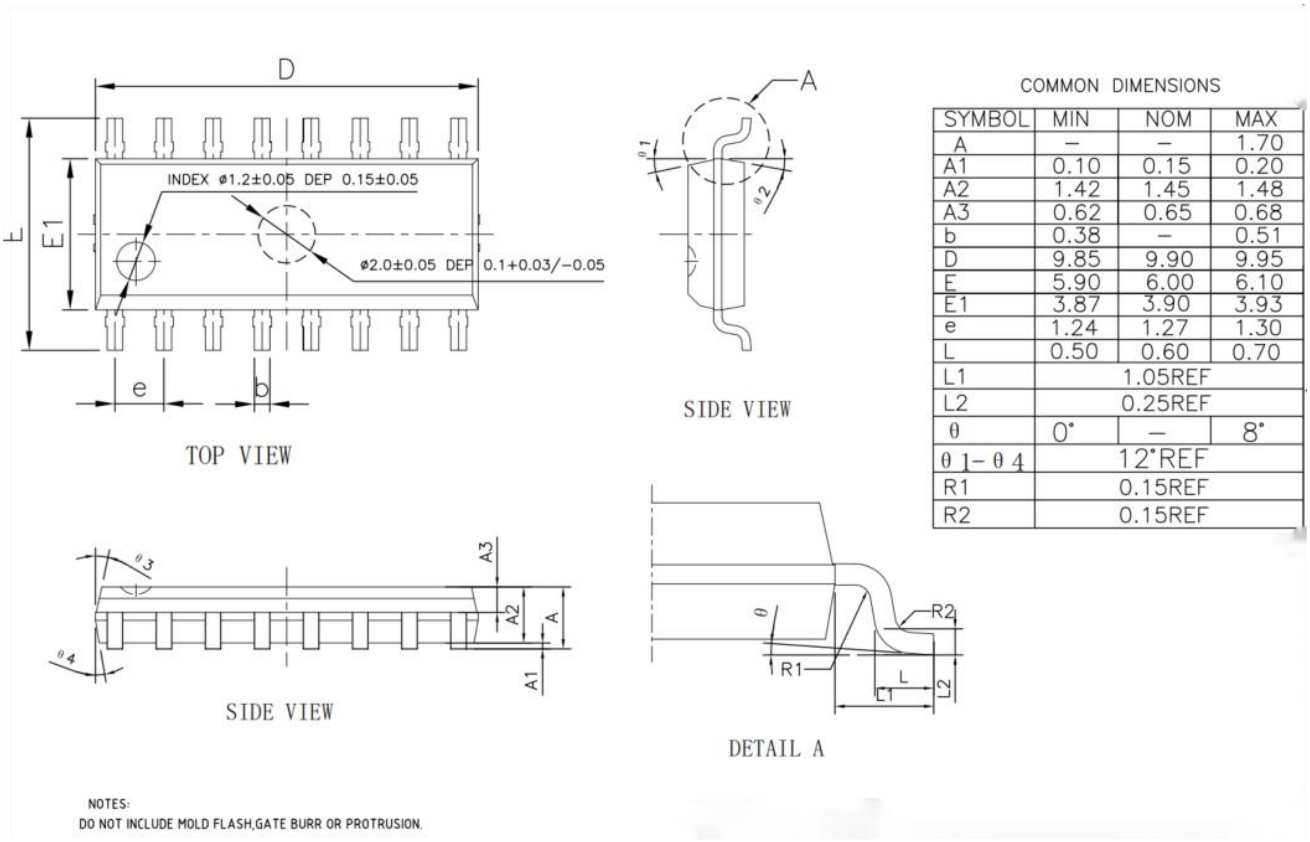
10.1 SSOP24



SYMBOL	MIN	NOM	MAX
A	–	–	1.70
A1	0.10	0.15	0.20
A2	1.40	1.45	1.50
A3	0.62	0.65	0.68
b	0.23	0.25	0.28
D	8.53	8.63	8.73
E	5.90	6.00	6.10
E1	3.80	3.90	3.95
e		0.635BSC	
L	0.50	0.60	0.70
L1	–	1.05REF	–
L2	–	0.25BSC	–
θ	0°	–	8°
θ1	11°	12°	13°
θ2	11°	12°	13°
θ3	11°	12°	13°
θ4	11°	12°	13°

Figure 17: SSOP24 Package Dimensions

10.2 SOP16

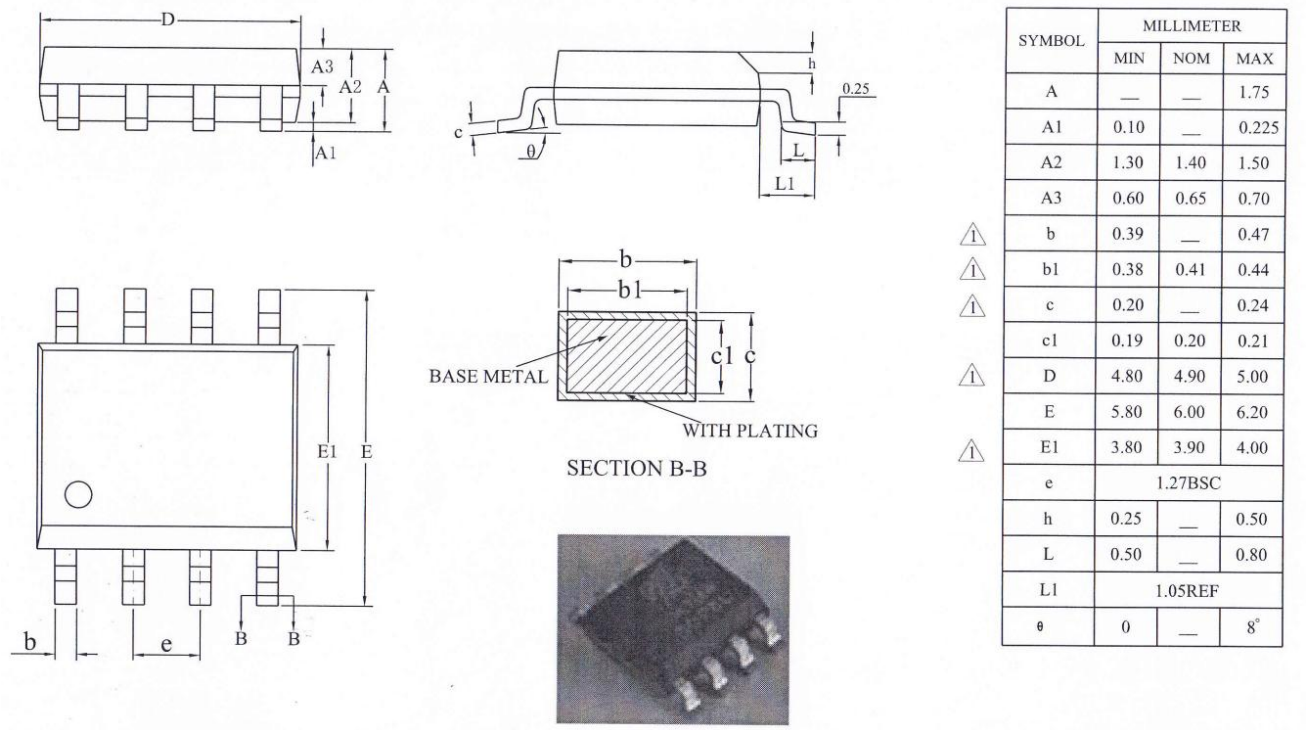


COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX
A	—	—	1.70
A1	0.10	0.15	0.20
A2	1.42	1.45	1.48
A3	0.62	0.65	0.68
b	0.38	—	0.51
D	9.85	9.90	9.95
E	5.90	6.00	6.10
E1	3.87	3.90	3.93
e	1.24	1.27	1.30
L	0.50	0.60	0.70
L1	1.05REF		
L2	0.25REF		
θ	0°	—	8°
θ1−θ4	12°REF		
R1	0.15REF		
R2	0.15REF		

Figure 18: SOP16 Package Dimensions

10.3 SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
1 b	0.39	—	0.47
1 b1	0.38	0.41	0.44
1 c	0.20	—	0.24
c1	0.19	0.20	0.21
1 D	4.80	4.90	5.00
E	5.80	6.00	6.20
1 E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 19: SOP8 Package Dimensions

11 Sample Application and Layout Guide

11.1 Sample Application

11.1.1 SSOP24

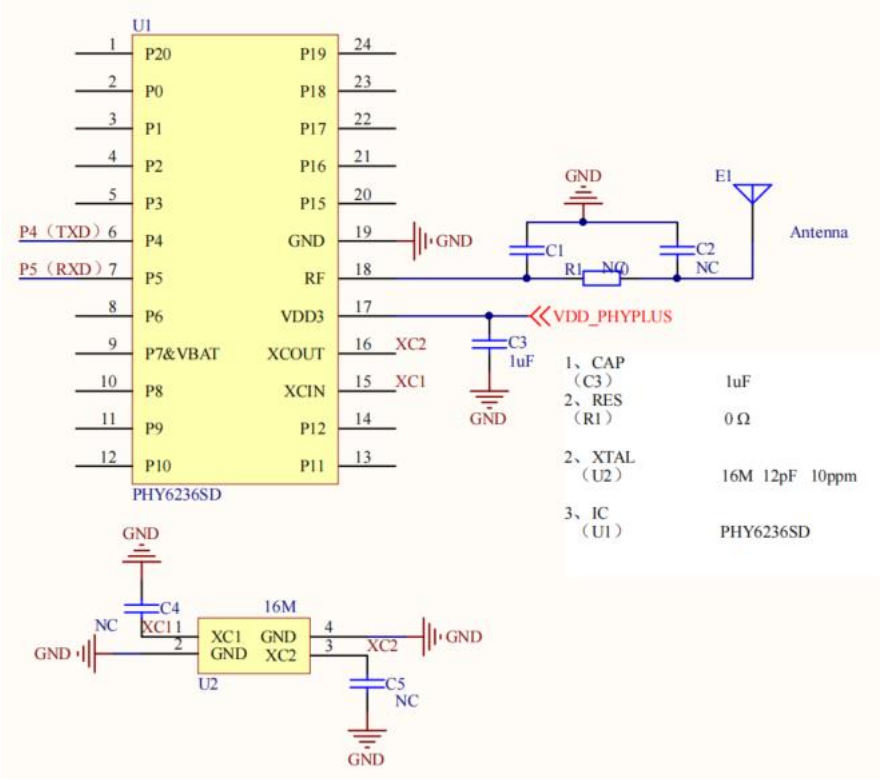


Figure 20: Sample Application of SSOP24

11.1.2 SOP16

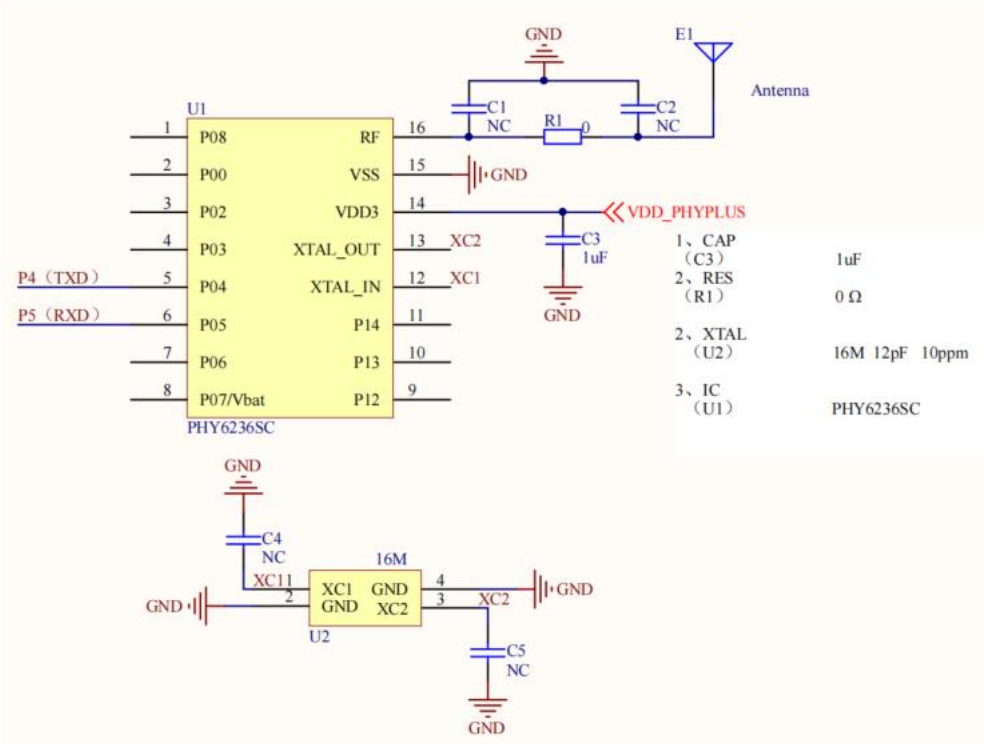


Figure 21: Sample Application of SOP16

11.1.3 SOP8

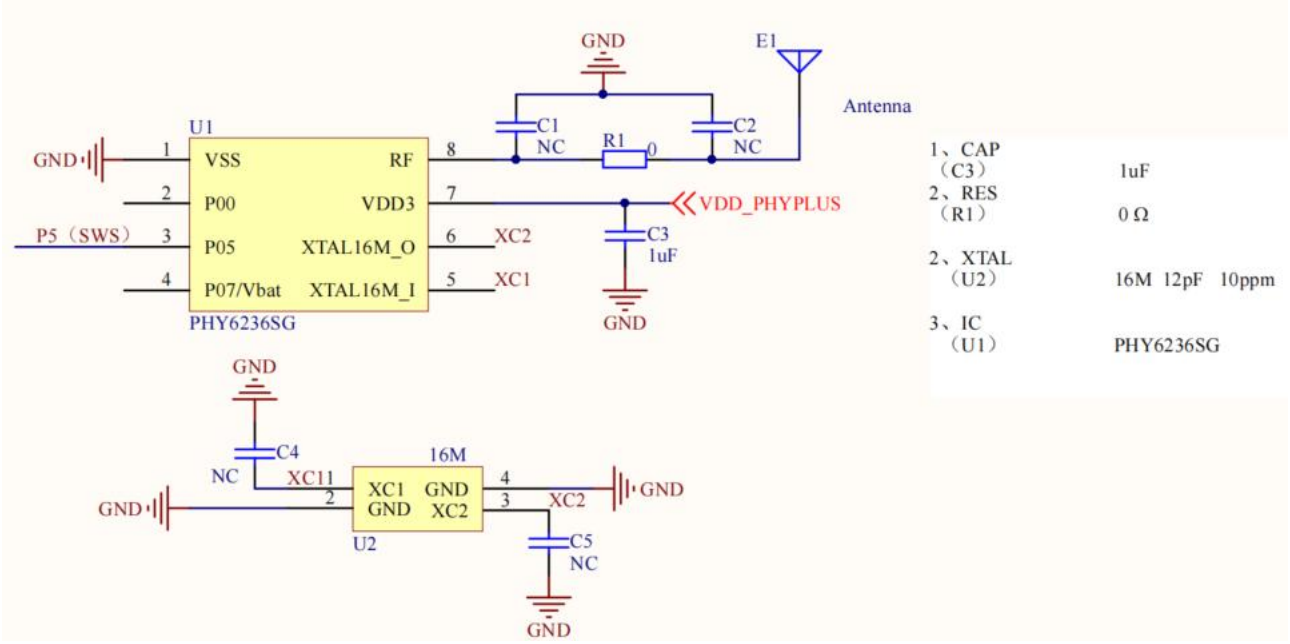


Figure 22: Sample Application of SOP8

11.2 Layout Guide

11.2.1 Placement

1. RF matching/Loop filter leading to antenna should be isolated from any other AC/DC signal as much as possible;
2. Xtal/OSC clock is a noise source to other circuits, keep clock trace as short as possible and away from any important area;
3. LDO's are sensitive and could be easily contaminated, care should be taken for the environment;
4. Antenna is the main RF radiation point, other important blocks should be shielded or away from this area.

RF traces

1. Define RF line width with given dielectric thickness (thickness of PCB dielectric layer to ground plain) to achieve 50ohm impedance; this is mainly for the RF line connecting to matching/loop filter and antenna.
2. Differential traces should be kept in the same length and component should be placed symmetrically;
3. Certain length of RF trace should be treated as part of RF matching.

11.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to the pin.
4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

11.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be "Ground " layer , for both signal ground and RF reference ground , DO NOT put any other trace or plane on second layer, otherwise "antenna effect" will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for "signal " layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

11.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

11.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.
2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace , the strong clock or RF signal would travel with power line.

11.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible , too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.