Single-chip USB to UART Bridge CP2102C Data Sheet

The CP2102C devices are designed to quickly add USB to your applications by eliminating firmware complexity and reducing development time.

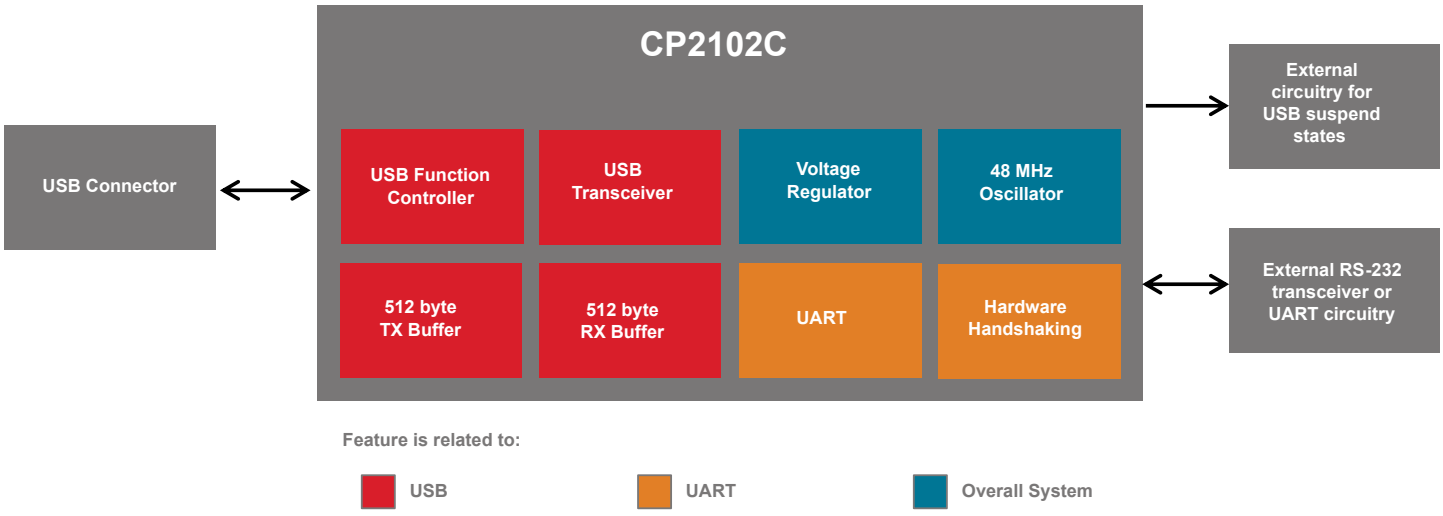
These highly-integrated USB-to-UART bridge controllers provide a simple solution for updating RS-232 designs to USB using a minimum of components and PCB space. CP2102C includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and Universal Asynchronous Receiver/Transmitter (UART) in packages as small as 4 mm x 4 mm. No other external USB components are required for development. No support for customizing device's configuration. By eliminating the need for complex firmware, CP2102C devices enable quick USB connectivity with minimal development effort.

CP2102C is ideal for a wide range of applications, including the following:

- POS terminals
- USB dongles
- Gaming controllers
- Medical equipment
- Data loggers

KEY FEATURES

- No firmware development required
- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- USB 2.0 full-speed compatible
- Data transfer rates up to 3 Mbaud
- Low operating current : 9.5 mA
- Standard CDC drivers - no custom driver needed.



1. Feature List and Ordering Information

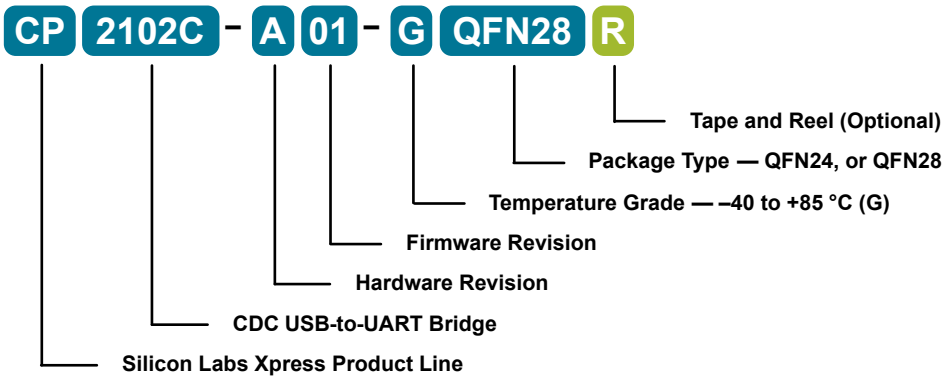


Figure 1.1. CP2102C Part Numbering

The CP2102C devices have the following features:

- **Single-Chip USB-to-UART Data Transfer**
  - Integrated USB transceiver; no external resistors required
  - Integrated clock; no external crystal required
  - On-chip power-on reset circuit
  - On-chip voltage regulator — 3.3 V output
- **USB Function Controller**
  - USB Specification 2.0 compliant; full-speed (12 Mbps)
  - USB suspend states supported via SUSPEND pins
- **USB communication device class**
  - Standard USB CDC requires no custom driver
  - Works with existing COM port Applications
  - Supported on Windows, Mac, and Linux
- **Single power supply of 3.0 to 3.6 V or 3.0 to 5.25 V**
- **Universal Asynchronous Receiver/Transmitter (UART)**
  - All handshaking and modem interface signals
  - Data formats supported
    - Data bits — 5, 6, 7, and 8
    - Stop bits — 1, 1.5, and 2
    - Parity — odd, even, mark, space, no parity
  - Baud rates: 300 baud to 3 Mbaud
  - 512 byte receive buffer
  - 512 byte transmit buffer
  - Hardware handshaking supported

Table 1.1. Product Selection Guide

Ordering Part Number	GPIOs	Battery Charger Detect	Separate VIO and VDD Pins	Pb-free (RoHS Compliant)	Temperature Range	Package
CP2102C-A01-GQFN28	0	—	—	Yes	-40 to +85 °C	QFN28
CP2102C-A01-GQFN24	0	—	Yes	Yes	-40 to +85 °C	QFN24

Note:

1. Devices with the same ordering part number may have different types of pin 1 indicators. However, all of these variants can use the same landing diagram as long as the recommended landing diagram instructions are followed

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2. Typical Connection Diagrams

2.1 Power

In all cases, a 1 kΩ pull-up on the RSTb pin is recommended. This pull-up should be tied to VIO on devices that have it. On devices where VIO is connected to VDD or devices that do not have VIO, this pull-up should be tied to VDD. The RSTb pin will be driven low during power-on and power failure reset events.

The figure below shows a typical connection diagram for the power pins of the CP2102C devices when the internal regulator is used and USB is connected (bus-powered).

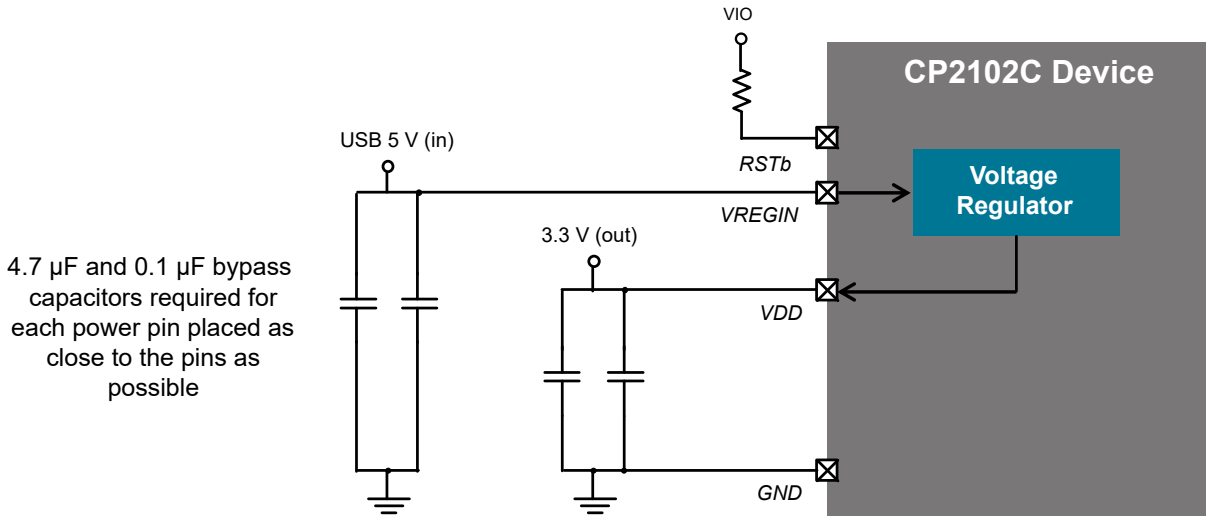

Figure 2.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

The figure below shows a typical connection diagram for the power pins of the CP2102C devices when the internal regulator is used and USB is connected (self-powered).

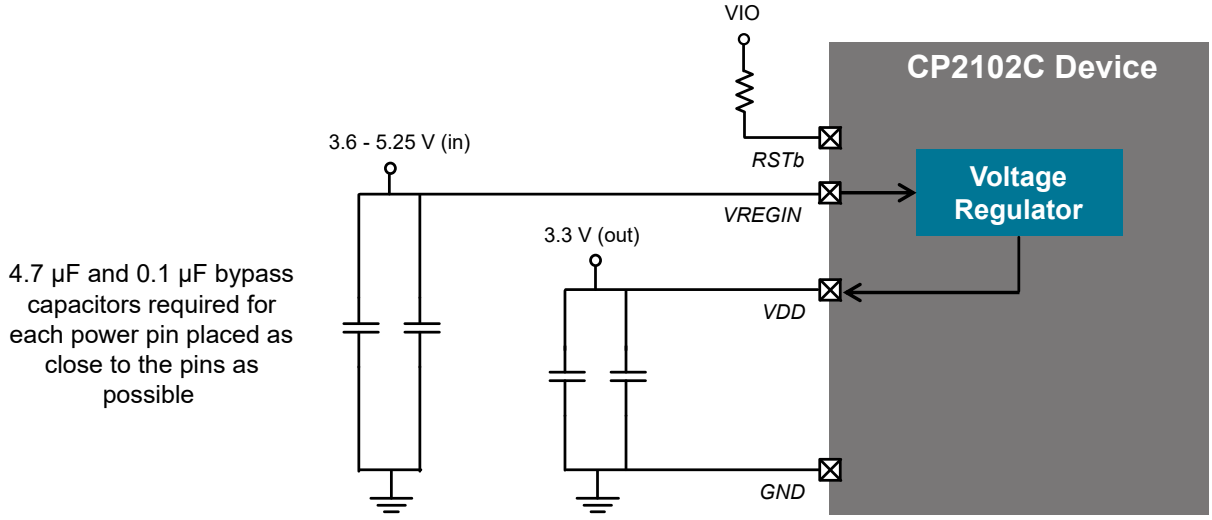

Figure 2.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the CP2102C devices when the internal 5 V-to-3.3 V regulator is not used.

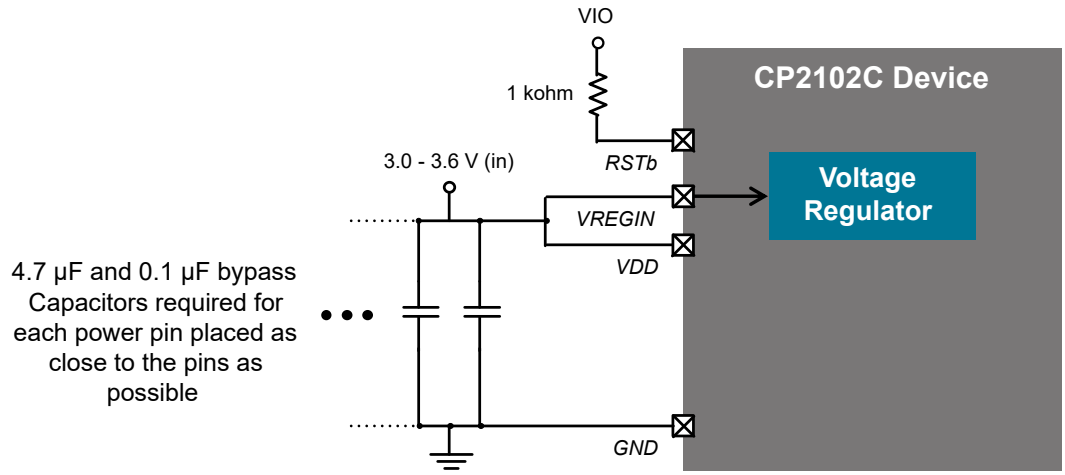

Figure 2.3. Connection Diagram with Voltage Regulator Not Used

2.2 USB

The figure below shows a typical connection bus-powered diagram for the USB pins of the CP2102C devices including ESD protection diodes on the USB pins.

Note: There are two relevant restrictions on the VBUS pin voltage in self-powered and bus-powered configurations. The first is the absolute maximum voltage on the VBUS pin, which is defined as VIO + 2.5 V in Table 3.9 Absolute Maximum Ratings on page 12. The second is the Input High Voltage (VIH) for VBUS to detect when the device is connected to a bus, which is defined as VIO – 0.6 V in Table 3.6 UART and Suspend I/O DC Electrical Characteristics on page 10. A resistor divider (or functionally-equivalent circuit) on VBUS is required to meet these specifications and ensure reliable device operation. In this case, the current limitation of the resistor divider prevents high VBUS pin leakage current, even though the VIO + 2.5 V specification is not strictly met while the device is not powered.

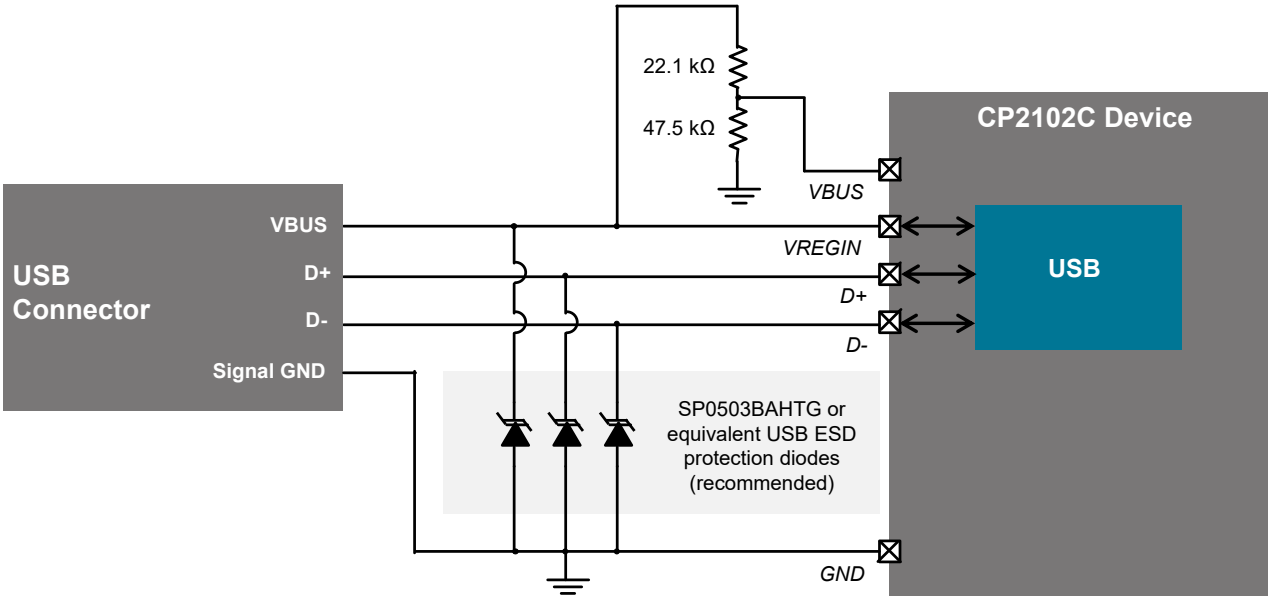

Figure 2.4. Bus-Powered Connection Diagram for USB Pins

The figure below shows a typical connection self-powered diagram for the USB pins of the CP2102C devices including ESD protection diodes on the USB pins.

Note: There are two relevant restrictions on the VBUS pin voltage in self-powered and bus-powered configurations. The first is the absolute maximum voltage on the VBUS pin, which is defined as VIO + 2.5 V in Table 3.9 Absolute Maximum Ratings on page 12. The second is the Input High Voltage (VIH) for VBUS to detect when the device is connected to a bus, which is defined as VIO – 0.6 V in Table 3.6 UART and Suspend I/O DC Electrical Characteristics on page 10. A resistor divider (or functionally-equivalent circuit) on VBUS is required to meet these specifications and ensure reliable device operation. In this case, the current limitation of the resistor divider prevents high VBUS pin leakage current, even though the VIO + 2.5 V specification is not strictly met while the device is not powered.

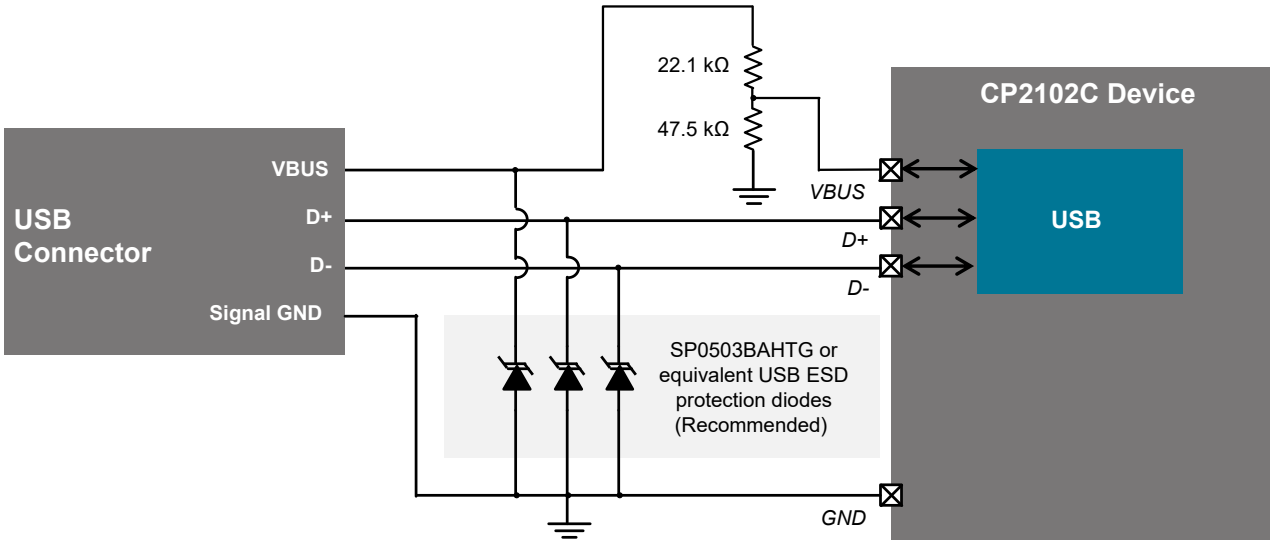

Figure 2.5. Self-Powered Connection Diagram for USB Pins

3. Electrical Specifications

3.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1 Recommended Operating Conditions on page 8, unless stated otherwise.

3.1.1 Recommended Operating Conditions

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		3.0	—	3.6	V
Operating Supply Voltage on VIO [3]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN	V_{REGIN}		3.0	—	5.25	V
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. I/O levels are undefined whenever VIO is less than 1 V.

3.1.2 Power Consumption

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal Operation[1, 2]	I_{DD}	115200 baud transmitting continuous bidirectional data	—	9.5	—	mA
		3 Mbaud transmitting continuous bidirectional data	—	13.7	—	mA
USB Suspend[1, 2]	I_{DD}		—	195	—	µA
Held in Reset[1, 2]	I_{DD}		—	1.3	—	mA
USB Pull-up[3]	I_{PU}		—	200	230	µA

Note:

1. Includes supply current from internal LDO regulator, supply monitor, and internal oscillators. These power consumption numbers are only for the CP2102C and do not include an external RS232 transceiver or other external circuitry.
2. USB Pull-up current should be added for total supply current. Normal and suspended supply current is current flowing into VREGIN.
3. The USB Pull-up supply current values are calculated values based on USB specifications. USB Pull-up supply current is current flowing from VDD to GND through USB pull-down/pull-up resistors on D+ and D-.

3.1.3 Reset and Supply Monitor

Table 3.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.2	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.2 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RSTb Low Time to Generate Reset	t_{RSTL}		15	—	—	µs

Note:
1. The RSTb pin will be driven low during power-on and power failure reset events.

3.1.4 Internal Oscillator

Table 3.4. Internal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Oscillator Frequency	f_{OSC}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{OSC}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{OSC}	V_{DD} = 3.0 V	—	45	—	ppm/°C

3.1.5 5 V Voltage Regulator

Table 3.5. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range [1]	V_{REGIN}		3.0	—	5.25	V
Output Voltage on VDD [2]	V_{REGOUT}	Output Current = 1 to 100 mA Regulation range (VREGIN ≥ 4.1V)	3.1	3.3	3.6	V
		Output Current = 1 to 100 mA Dropout range (VREGIN < 4.1V)	—	V_{REGIN} – $V_{DROPOUT}$	—	V
Output Current [2]	I_{REGOUT}		—	—	100	mA
Dropout Voltage	$V_{DROPOUT}$	Output Current = 100 mA	—	—	0.8	V

Note:

1. Input range to meet the Output Voltage on VDD specification. If the 5 V voltage regulator is not used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

3.1.6 UART and Suspend I/O DC Electrical Characteristics

Table 3.6. UART and Suspend I/O DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 3.6 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Input High Voltage	V_{IH}		V_{IO} - 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.0 V	0	5	150	µA

3.1.7 USB Transceiver

Table 3.7. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmitter						
Output High Voltage	V_{OH}	$V_{DD} \geq 3.0V$	2.8	—	—	V
Output Low Voltage	V_{OL}	$V_{DD} \geq 3.0V$	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	28	36	44	Ω
		Driving Low	28	36	44	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
Output Rise Time	T_R	Full Speed	4	—	20	ns
Output Fall Time	T_F	Full Speed	4	—	20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

3.2 Thermal Conditions

Table 3.8. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	QFN24 Packages	—	30	—	°C/W
		QFN28 Packages	—	26	—	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	QFN24 Packages	—	24.2	—	°C/W
		QFN28 Packages	—	18.8	—	°C/W
Thermal Characterization Parameter (Junction to Top)	Ψ_{JT}	QFN24 Packages	—	0.3	—	°C/W
		QFN28 Packages	—	0.3	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

3.3 Absolute Maximum Ratings

Stresses above those listed in 3.3 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 3.9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO[2]	V_{IO}		GND-0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND-0.3	5.8	V
Voltage on D+ or D-	V_{USBD}		GND-0.3	V_{DD}+0.3	V
Voltage on UART pins, VBUS, RSTb, or any other non-power, non-USB pin	V_{IN}	V_{IO} > 3.3 V	GND-0.3	5.8	V
		V_{IO} < 3.3 V	GND-0.3	V_{IO}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any UART pins, VBUS, RSTb, or any other non-power, non-USB pin	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J		-40	105	°C

Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. On devices without a VIO pin, $V_{IO} = V_{DD}$

3.4 Typical Performance Curves

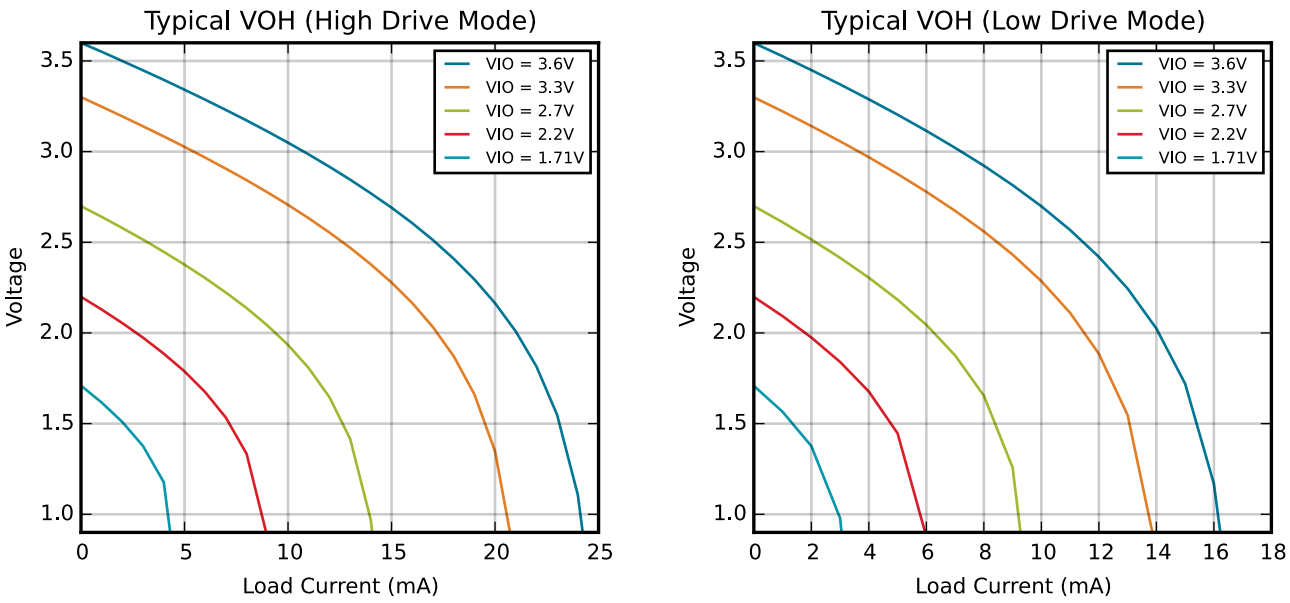

Figure 3.1. Typical V_{OH} Curves

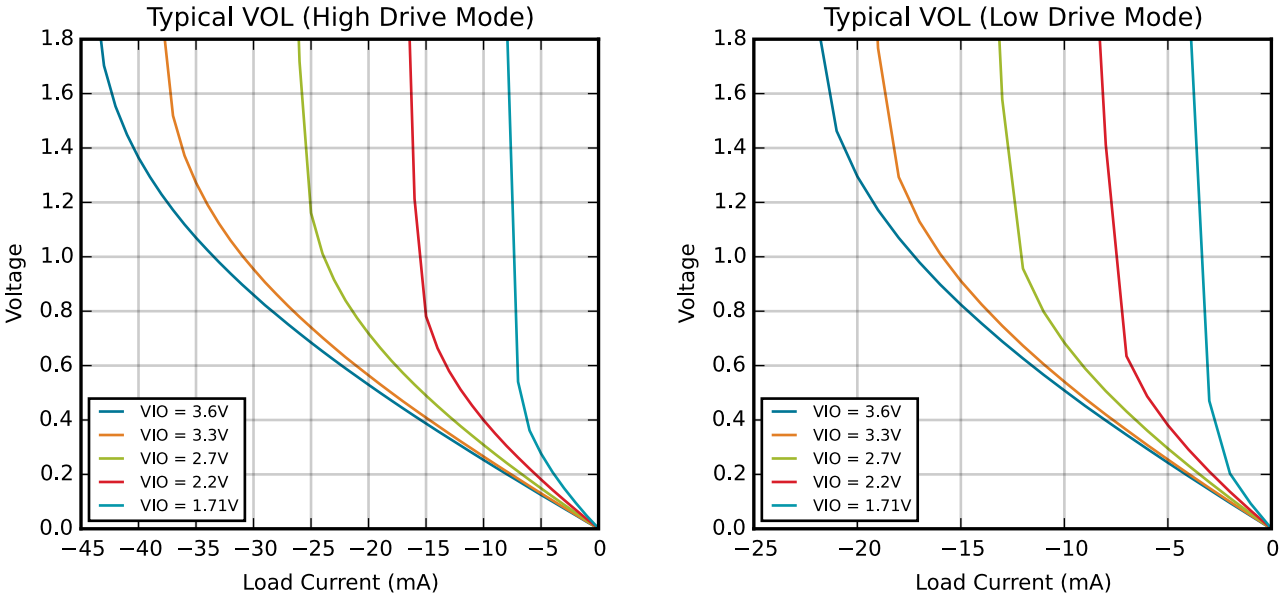

Figure 3.2. Typical V_{OL} Curves

4. Functional Description

4.1 USB Function Controller and Transceiver

The Universal Serial Bus function controller in the CP2102C is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pull-up resistors. The USB function controller manages all data transfers between the USB and the UART as well as command requests generated by the USB host controller and commands for controlling the function of the UART.

The USB Suspend and Resume signals are supported for power management of both the CP2102C device as well as external circuitry. The CP2102C will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the CP2102C asserts the SUSPEND and SUSPENDb signals. SUSPEND and SUSPENDb are also asserted after a CP2102C reset until device configuration during USB Enumeration is complete.

The CP2102C exits Suspend mode when any of the following occur:

1. Resume signaling is detected or generated.
2. A USB Reset signal is detected.
3. A device reset occurs.

On exit of Suspend mode, the SUSPEND and SUSPENDb signals are de-asserted. Both SUSPEND and SUSPENDb temporarily float high during a CP2102C reset. If this behavior is undesirable, a strong pull-down (10 kΩ) can be used to ensure SUSPENDb remains low during reset.

4.2 Universal Asynchronous Receiver/Transmitter (UART) Interface

The CP2102C UART interface consists of the TX (transmit) and RX (receive) data signals as well as the RTS, CTS, DSR, DTR, DCD, and RI control signals. The UART supports DSR/DTR and RTS/CTS handshaking.

The UART is programmable to support a variety of data formats and baud rates. The data formats and baud rates available are listed in the table below.

Table 4.1. Data Formats and Baud Rates

Parameter	Available Values
Data Bits	5, 6, 7, and 8
Stop Bits	1, 1.5[1], and 2
Party Types	none, even, odd, mark, space
Baud Rates	300, 600, 1200, 1800, 2400, 4000, 4800, 7200, 9600, 14400, 16000, 19200, 28800, 38400, 51200, 56000, 57600, 64000, 76800, 115200, 128000, 153600, 230400, 250000, 256000, 460800, 500000, 576000, 921600, 1000000, 1200000, 1500000, 2000000, 3000000

Note:
1. 5-bit only.

4.2.1 Baud Rate Generation

The baud rate generator is very flexible, allowing the user to request any baud rate in the range from 300 baud to 3 Mbaud. If the baud rate cannot be directly generated from the 48 MHz oscillator, the device will choose the closest possible option. The actual baud rate is dictated by the following equations.

$$\text{Clock Divider} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Requested Baud Rate}}$$

$$\text{Actual Baud Rate} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Clock Divider}}$$

In both cases, the Prescale value is 4 if the Requested Baud Rate is ≤ 365 baud and 1 if the Requested Baud Rate value is > 365 baud.

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than ±2%. The Clock Divider value is rounded to the nearest integer, which may produce an error source. Another error source will be the 48 MHz oscillator, which is accurate to ±0.25%. Knowing the actual and requested baud rates, the total baud rate error can be found using the equation below.

$$\text{Baud Rate Error (\%)} = 100 \times \left(1 - \frac{\text{Actual Baud Rate}}{\text{Requested Baud Rate}}\right) \pm 0.25\%$$

4.2.2 Sending Break Signaling

The CP2102C supports break signaling with an external 10k Ohm resistor between TXD and ground. This resistor is sufficient for break signaling across all baud rates.

When a Send Break command is received, the CP2102C halts adding new data to the transmitter FIFO and will wait 6 byte times for in-flight data to complete transmission. It will not process other USB transactions such as RX data reception while waiting - transactions will be processed once break is initiated. If RTS TX Control is enabled, RTS will also begin asserting. Once the 6 byte time has expired, the CP2102C places the TXD line in a high-impedance state - ignoring flow control status - and the external resistor pulls down TXD to initiate a break.

While sending break, USB transactions including RX data reception normally.

When a Stop Break command is received, the CP2102C removes TXD from the high impedance state. It is held for 1 byte time to allow for stabilization. After that time has expired the transmitter resumes normal operations, and RTS (if RTS TX Control is enabled) signals wait the specified hold time.

4.3 Additional Features

4.3.1 Hardware Handshaking (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2102C, the device must be configured to use hardware flow control on the USB host.

RTS, or Ready To Send, is an active-low output from the CP2102C and indicates to the external UART device that the CP2102C's UART RX FIFO has not reached the FLOW OFF watermark level of 448 bytes and is ready to accept more data. When the amount of data in the RX FIFO reaches the watermark, the CP2102C pulls RTS high to indicate to the external UART device to stop sending data. The CP2102C does not pull RTS low again until the UART RX FIFO is at the FLOW ON watermark level of 384 bytes (at least 128 free bytes). This hysteresis allows for optimal operation.

Note: RTS TX Control signaling is a special mode that asserts RTS while the CP2102C is transmitting. This mode is not available below 300 baud. RTS hardware flow control works at all baud rates.

CTS, or Clear To Send, is an active-low input to the CP2102C and is used by the external UART device to indicate to the CP2102C when the external UART device's RX FIFO is getting full. The CP2102C will not send more than two bytes of data once CTS is pulled high.

Hardware handshaking allows for optimal continuous transmission speeds at high baud rates (greater than 1 MBaud). The effective throughput depends on USB bus loading and host USB stack efficiency. The typical maximum continuous bidirectional data transfer is > 450 kbytes/s at 3 Mbaud.

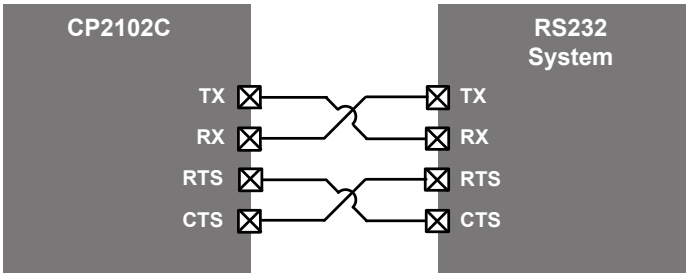

Figure 4.1. Using Hardware Flow Control with the CP2102C

4.3.2 Data Throughput Optimization

Effective throughput depends on several factors:

- CP2102C placement on the physical USB device tree
- USB bus load from other devices
- Host OS USB stack efficiency
- CP2102C configuration options

Handshaking is required at high baud rates (greater than 1 MBaud) to avoid receiver overrun. A request to stop transmission is only initiated once the RX FIFO has reached the FLOW OFF watermark level. Once the USB bus lowers the RX FIFO level below the FLOW ON watermark, a request to continue transmission is sent.

Hardware handshaking allows for optimal continuous transmission speeds at high baud rates. Using a Windows host PC, the CP2102C's typical maximum continuous bidirectional throughput is > 450 kbytes/s at 3 Mbaud (> 70% efficiency).

For these performance numbers, the CP2102C is placed on a USB hub connected to the Windows host PC with a third party UART adapter. The only significant USB traffic is generated by the USB to UART devices. The Windows host PC is running automated tests with minimal CPU load.

Certain conditions will reduce the maximum throughput at high baud rates (> 1Mbaud):

- Using DSR, DTR, or DCD handshaking signals lowers maximum performance. Use hardware CTS/RTS only for peak performance.
- Embedded events or error character insertion requires free space in the UART RX FIFO to post events to the host. At high baud rates with continuous data reception, this space may not be available. Limit maximum baud rates with continuous data reception to 1 MBaud when using embedded events or error character insertion to guarantee reception of events or the error character.
- Transmitting an immediate character momentarily causes lower bidirectional throughput as the character forces a bypass of the current transmit FIFO. Once the character has been transmitted, the typical bidirectional throughput is restored.

4.3.3 Modem Control (DSR, DTR, DCD, RI)

The modem control pins are enabled when requested on the host, it is controlled by the operating system's CDC driver.

Note: Mac doesn't support modem control.

Table 4.2. Modem Control Signals

Modem Control Signal	Description
DSR	Input to the CP2102C. Data Set Ready control input (active low).
DTR	Output from the CP2102C. Data Terminal Ready control output (active low). Note that this pin may toggle when opening a COM port on some operating systems.
DCD	Input to the CP2102C. Data Carrier Detect control input (active low).
RI	Input to the CP2102C. Ring Indicator control input (active low).

4.3.4 Receiver Timeout

The CP2102C supports a new custom vendor command to configure the internal buffer receive timeout. During normal operation, when data is received the receive buffer waits up to 2 ms or 128 character times, whichever is fewer, before transferring data to host. This timer is reset each time new data is received. For some usage models, this response time causes unwanted extra latency between receiving a byte at the UART and the byte being available on the host. The Set Receiver Max Timeout custom vendor command allows applications to set the timeout from .001 ms to 2 ms. Small values will cause the receiver to inefficiently use the 512 byte Receive Buffer and should not be used at high data rates (greater than 230400).

5. Pin Definitions

5.1 CP2102C QFN28 Pin Definitions

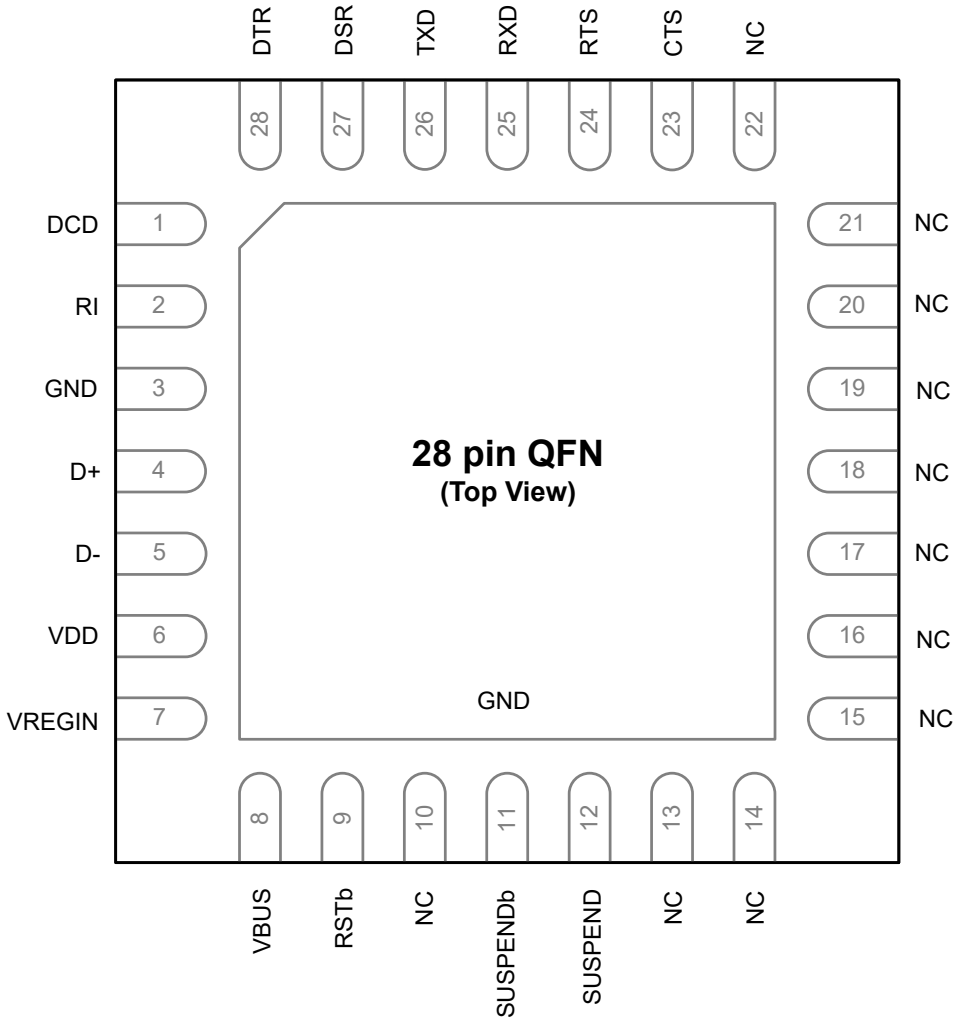

Figure 5.1. CP2102C QFN28 Pinout

Table 5.1. Pin Definitions for CP2102C QFN28

Pin Number	Pin Name	Description
1	DCD	Digital Input. Data Carrier Detect control input (active low).
2	RI	Digital Input. Ring Indicator control input (active low).
3	GND	Ground
4	D+	USB Data Positive
5	D-	USB Data Negative
6	VDD	Supply Power Input / Voltage Regulator Output
7	VREGIN	5V Regulator Input

Pin Number	Pin Name	Description
8	VBUS	Digital Input. VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network through a resistor divider as described in 2.2 USB. A 5 V signal on this pin indicates a USB network connection.
9	RSTb	Active-low Reset
10	NC	No Connect (leave this pin floating).
11	SUSPENDb	Digital Output. This pin is driven low when the device enters the USB suspend state.
12	SUSPEND	Digital Output. This pin is driven high when the device enters the USB suspend state.
13	NC	No Connect (leave this pin floating).
14	NC	No Connect (leave this pin floating).
15	NC	No Connect (leave this pin floating).
16	NC	No Connect (leave this pin floating).
17	NC	No Connect (leave this pin floating).
18	NC	No Connect (leave this pin floating).
19	NC	No Connect (leave this pin floating).
20	NC	No Connect (leave this pin floating).
21	NC	No Connect (leave this pin floating).
22	NC	No Connect (leave this pin floating).
23	CTS	Digital Input. Clear To Send control input (active low).
24	RTS	Digital Output. Ready To Send control output (active low).
25	RXD	Digital Input. Asynchronous data input (UART Receive).
26	TXD	Digital Output. Asynchronous data output (UART Transmit).
27	DSR	Digital Input. Data Set Ready control input (active low).
28	DTR	Digital Output. Data Terminal Ready control output (active low).
Center	GND	Ground

5.2 CP2102C QFN24 Pin Definitions

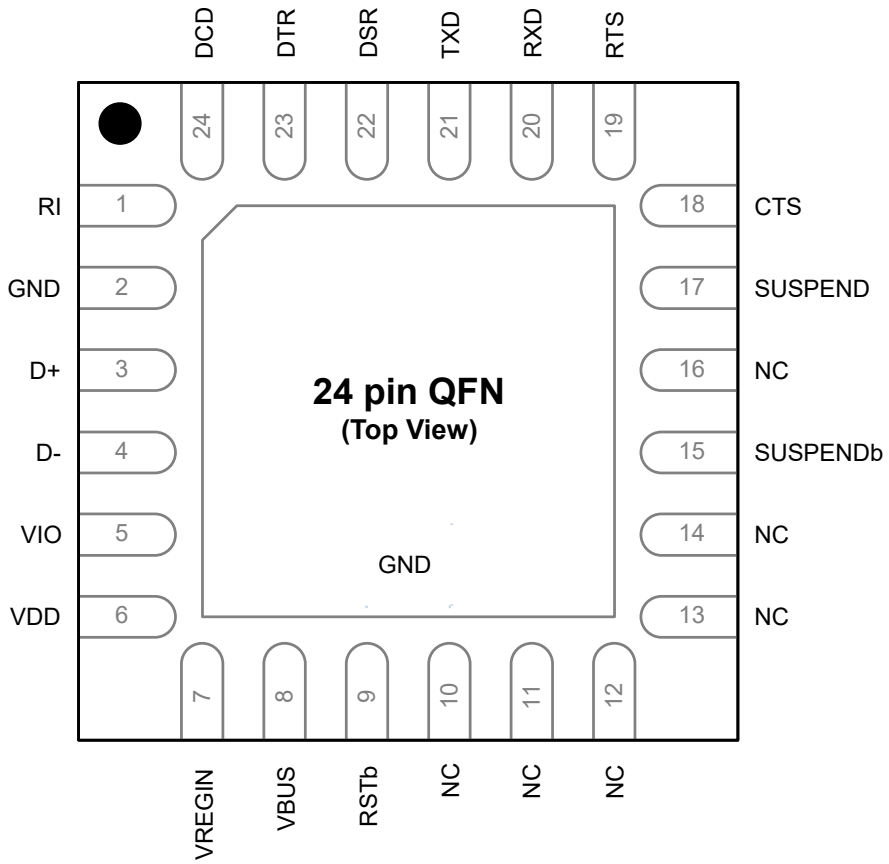

Figure 5.2. CP2102C QFN24 Pinout

Table 5.2. Pin Definitions for CP2102C QFN24

Pin Number	Pin Name	Description
1	RI	Digital Input. Ring Indicator control input (active low).
2	GND	Ground
3	D+	USB Data Positive
4	D-	USB Data Negative
5	VIO	I/O Supply Power Input
6	VDD	Supply Power Input / Voltage Regulator Output
7	VREGIN	5 V Regulator Input
8	VBUS	Digital Input. VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network through aresistor divider as described in 2.2 USB. A 5 V signal on this pin indicates a USB network connection.
9	RSTb	Active-low Reset
10	NC	No Connect (leave this pin floating).

Pin Number	Pin Name	Description
11	NC	No Connect (leave this pin floating).
12	NC	No Connect (leave this pin floating).
13	NC	No Connect (leave this pin floating).
14	NC	No Connect (leave this pin floating).
15	SUSPENDb	Digital Output. This pin is driven low when the device enters the USB suspend state.
16	NC	No Connect (leave this pin floating).
17	SUSPEND	Digital Output. This pin is driven high when the device enters the USB suspend state.
18	CTS	Digital Input. Clear To Send control input (active low).
19	RTS	Digital Output. Ready To Send control output (active low).
20	RXD	Digital Input. Asynchronous data input (UART Receive).
21	TXD	Digital Output. Asynchronous data output (UART Transmit).
22	DSR	Digital Input. Data Set Ready control input (active low).
23	DTR	Digital Output. Data Terminal Ready control output (active low).
24	DCD	Digital Input. Data Carrier Detect control input (active low).
Center	GND	Ground

6. QFN28 Package Specifications

6.1 QFN28 Package Dimensions

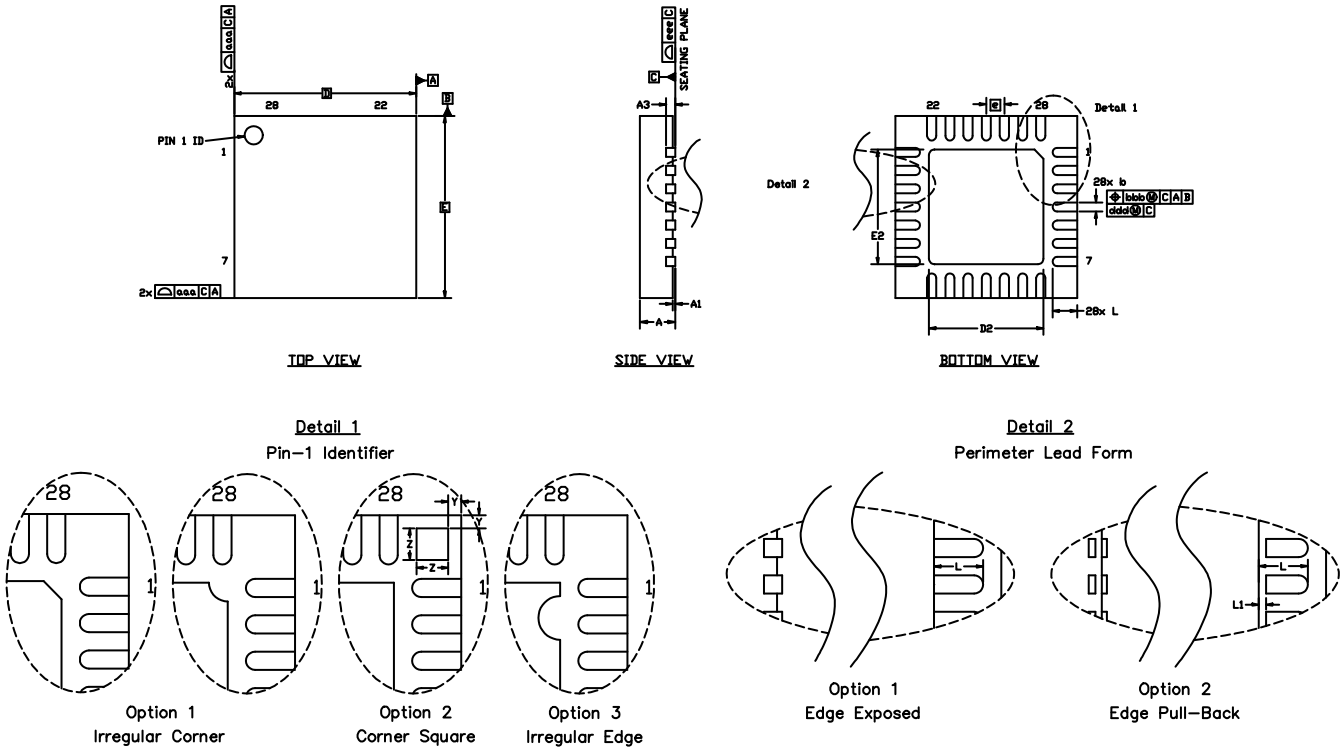

Figure 6.1. QFN28 Package Drawing

Table 6.1. QFN28 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		5.00 BSC	
D2	3.15	3.25	3.35
e		0.50 BSC	
E		5.00 BSC	
E2	3.15	3.25	3.35
L	0.45	0.55	0.65
aaa		0.10	
bbb		0.10	
ddd		0.05	

Dimension	Min	Typ	Max
eee		0.08	
Z		0.44	
Y		0.18	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220 except for custom features D2, E2, L, Z, and Y which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 QFN28 PCB Land Pattern

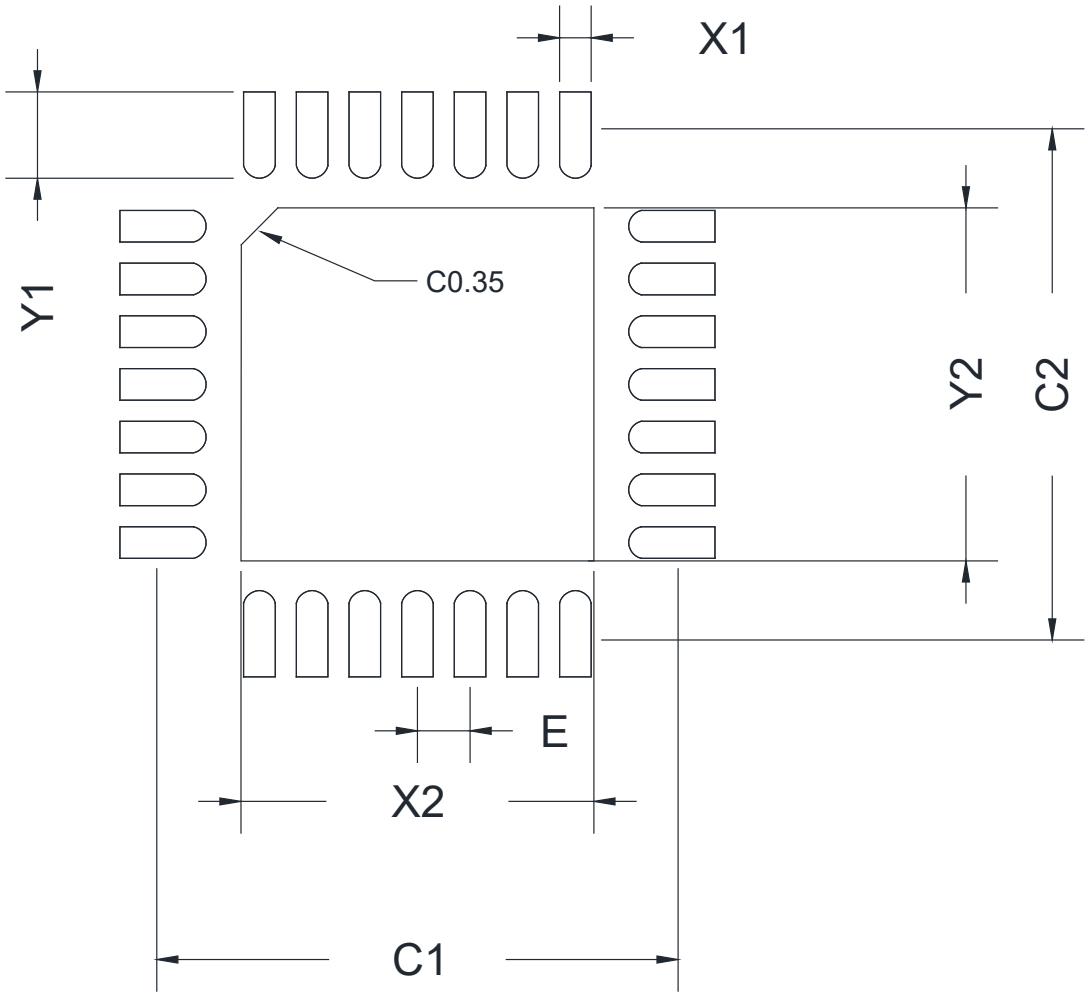

Figure 6.2. QFN28 PCB Land Pattern Drawing

Table 6.2. QFN28 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	
C2	4.80	
E	0.50	
X1	0.30	
X2	3.35	
Y1	0.95	
Y2	3.35	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.2 mm square openings on a 1.5 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3 QFN28 Package Marking

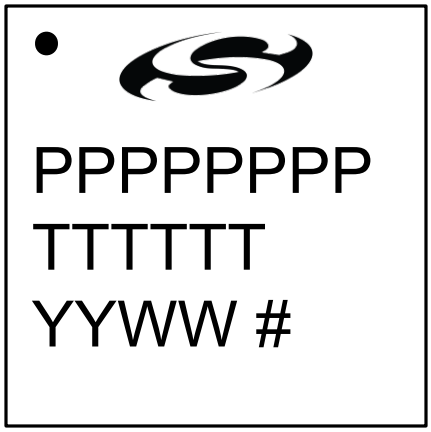

Figure 6.3. QFN28 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last two digits of the assembly year.
- WW – The two-digit workweek when the device was assembled.
- # – Indicates the hardware revision.

Note: Firmware revision is not part of the package marking.

7. QFN24 Package Specifications

7.1 QFN24 Package Dimensions

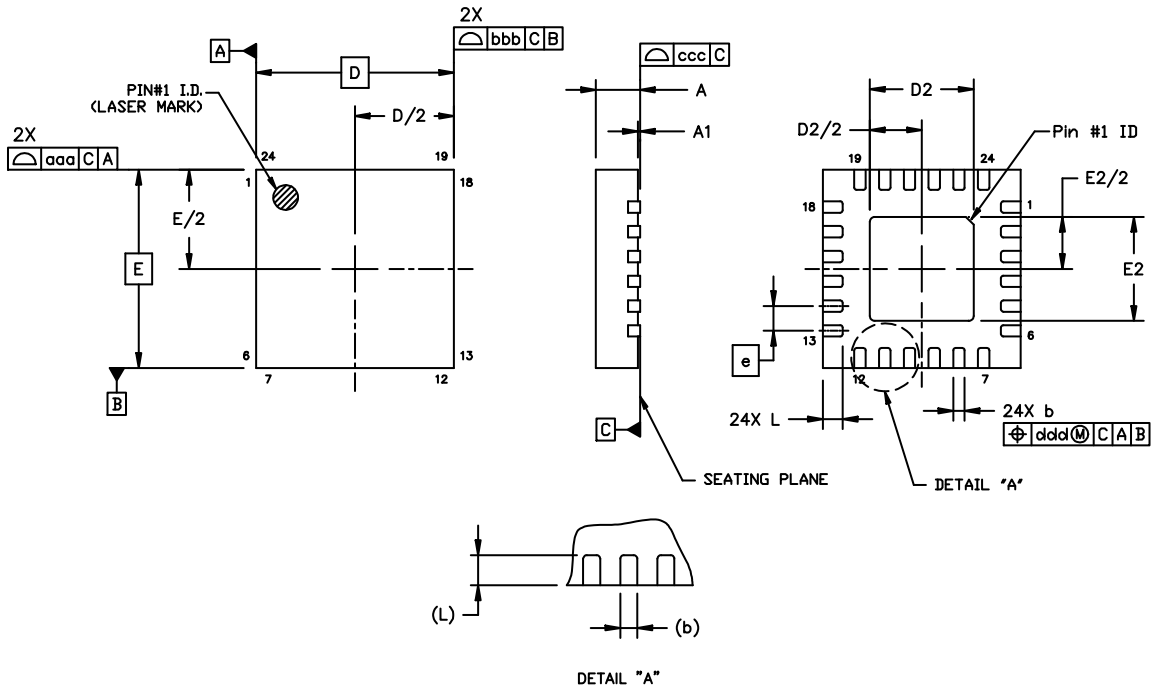

Figure 7.1. QFN24 Package Drawing

Table 7.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Dimension	Min	Typ	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 QFN24 PCB Land Pattern

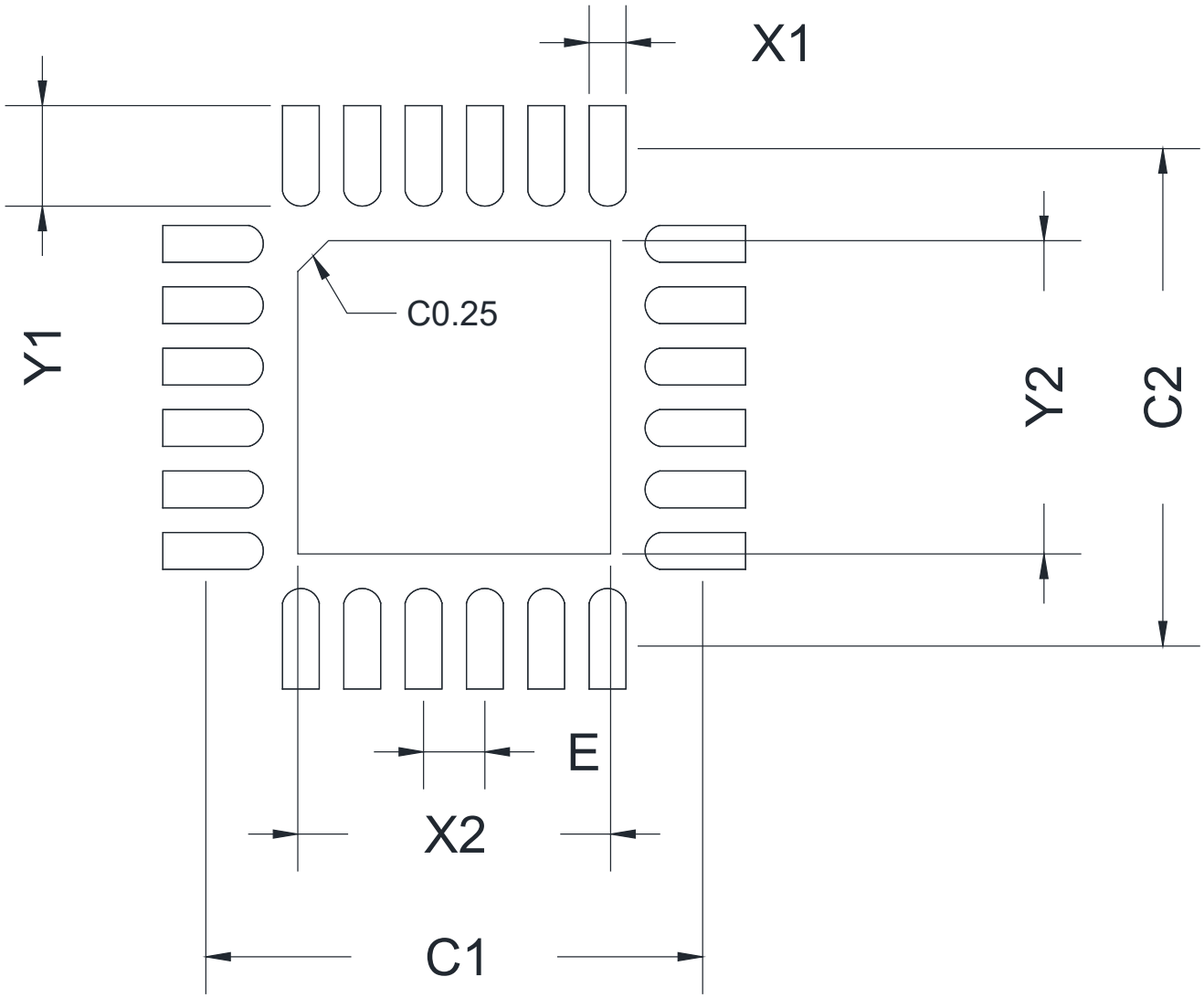

Figure 7.2. PCB Land Pattern Drawing

Table 7.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	
C2	3.90	
E	0.50	
X1	0.30	
X2	2.55	
Y1	0.85	
Y2	2.55	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 0.9 mm square openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN24 Package Marking

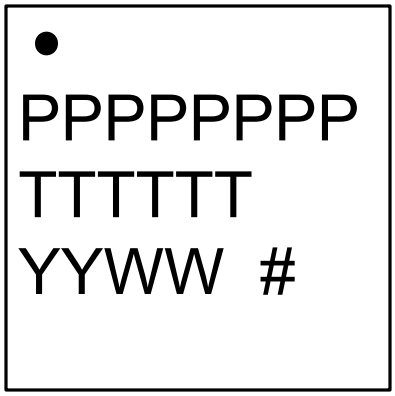

Figure 7.3. Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last two digits of the assembly year.
- WW – The two-digit workweek when the device was assembled.
- # – Indicates the hardware revision.

Note: Firmware revision is not part of the package marking.

8. Revision History

Revision 1.0

January 2025

- Initial release.

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