DATA SHEET

SKY66319-11: 4400 to 5000 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier

Applications

- TDD 4G LTE and 5G systems
- Driver amplifier for micro base stations and macro base stations
- Enterprise small-cell and massive MIMO

Features

- Wide instantaneous signal bandwidth: wider than 5x 20 MHz carrier
- High efficiency: PAE = 24% @ +28 dBm
- High linearity: +28 dBm with < –50 dBc ACLR with pre-distortion (100 MHz 5G, 8.5 dB PAR signal)
- High gain: 33 dB
- Excellent input and output return loss in 50 Ω systems
- Integrated active bias: Performance compensated over temperature
- Integrated enable ON/OFF function: PAEN = 1.5 to 2.5 V
- Single supply voltage: 5.0 V
- Pin-to-pin compatible PA family supporting major 3GPP bands
- Compact (16-pin, 5 x 5 x 1.3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

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Description

The SKY66319-11 is a highly efficient, wide instantaneous bandwidth, fully input/output matched power amplifier (PA) with high gain and linearity.

The compact 5 x 5 mm PA is designed for TDD 4G LTE and 5G systems operating from 4400 to 5000 MHz. The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.

The SKY66319-11 is part of high-efficiency, pin-to-pin compatible PA family supporting major 3GPP bands.

A block diagram is shown in Figure 1. The device package and pinout are shown in Figure 2. Table 1 lists the pin-to-pin compatible parts in the PA family. Signal pin assignments and functional pin descriptions are described in Table 2.

Table 1. Pin-to-Pin Compatible PA Family

Part Number	Frequency (MHz)	3GPP Band	Carrier Bandwidth (MHz)
SKY66312-11	2300 to 2400	n30, n40	100
SKY66317-11	2496 to 2690	B7, B38, n41	100
SKY66318-11	3300 to 3600	B42, n78	100
SKY66318-21	3300 to 3600	B42, B48, n78	200
SKY66320-11	3600 to 3800	B43, B48, n78	100
SKY66319-11	4400 to 5000	n79	100

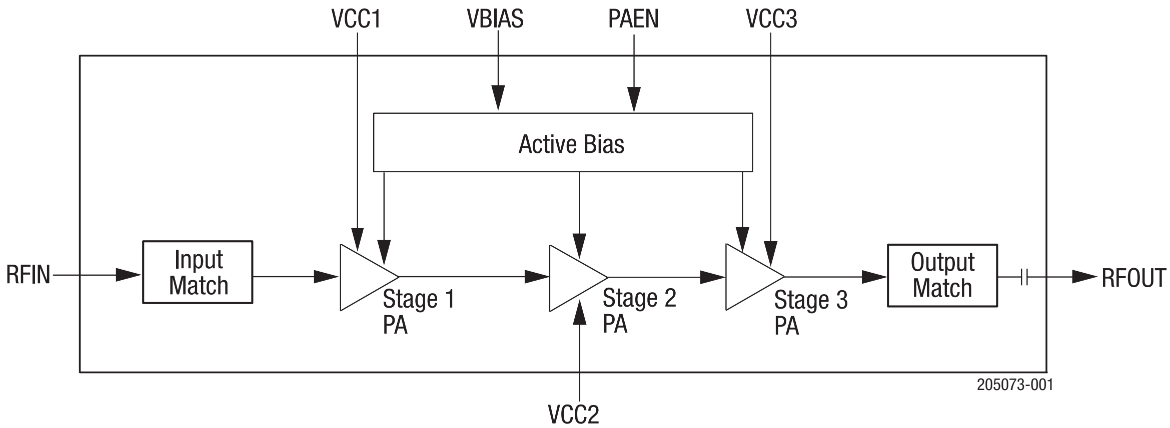


Figure 1. Block Diagram

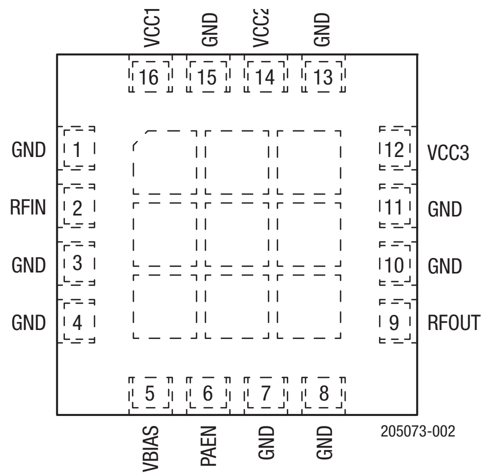


Figure 2. Pinout (Top View)

Table 2. Signal Descriptions[1]

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

1. The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY66319-11 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the VBIAS signal (pin 5).

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66319-11 are provided in Table 3. Recommended operating conditions are specified in Table 4, and electrical specifications are provided in Table 5.

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
RF input power (CW)	P_{IN}		+10	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC}		5.5	V
PA enable	V_{EN}		2.8	V
Operating temperature	T_C	–40	115	°C
Storage temperature	T_{ST}	–55	+125	°C
Junction temperature (for 10^6 hours MTTF)	T_J		+175	°C
Power dissipation (T_{CASE} = 110 °C P_{OUT} = +28 dBm)	P_D		3.12	W
Device thermal resistance (T_{CASE} = 110 °C P_{OUT} = +28 dBm)	q_{JC}		15	°C/W
RF turn-on/turn-off time[2]	t_{ON}/t_{OFF}		1	us
Electrostatic discharge Charged Device Model (CDM) Human Body Model (HBM)	ESD		 1 1	 kV kV

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.
2. RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state "on" level.
   RF turn-off time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power decreases to 10% of the average steady-state "on" level.

ESD Handling: *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC1}, V_{CC2}, V_{CC3}, V_{BIAS}	4.75	5	5.25	V
PA enable: ON OFF	PAEN	1.5 to 0.3	2.0 0	2.8 0.5	V
PA enable current	I_{ENABLE}		1	12	µA
Operating frequency	f	4400		5000	MHz
Operating temperature	T_C	–40	+25	+110	°C

Table 5. Electrical Specifications[1]
(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 4900 MHz, TC = +25 °C, Input/Output Load = 50 ohms, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		4800		5000	MHz
Small signal gain	$\|S_{21}\|$	P_{IN} = –30 dBm		35		dB
Gain @ +28 dBm	$\|S_{21}\|$@+28 dBm	P_{OUT} = +28 dBm CW	31.5	33.5		dB
Input return loss	$\|S_{11}\|$	P_{IN} = –20 dBm	10	20		dB
Output return loss	$\|S_{22}\|$	P_{IN} = –20 dBm	9	11		dB
Reverse isolation[2]	$\|S_{12}\|$	P_{IN} = –30 dBm		50		dB
Adjacent channel leakage ratio (100 MHz offset, open loop)[2]	ACLR100MHz	Pout = +28 dBm (100 MHz LTE, 8.5 dB PAR, 100 MHz offset)		–28	–26	dBc
Adjacent channel leakage ratio (20 MHz offset, open loop)	ACLR20MHz	Pout = +28 dBm (100 MHz LTE, 8.5 dB PAR, 20 MHz offset)		–26.6	–24.5	dBc
Saturated output power	P_{SAT}	CW, PIN = +6 dBm		+35.4		dBm
2nd harmonic[2]	$2f_O$	CW, P_{OUT} = +28 dBm		–43		dBc
3rd harmonic[2]	$3f_O$	CW, P_{OUT} = +28 dBm		–55		dBc
Power-added efficiency	PAE	CW, P_{OUT} = +28 dBm		24		%
Quiescent current	Iccq	No RF signal		100		mA

1. Performance is guaranteed only under the conditions listed in this table.
2. Not tested in production. Verified by design.

Typical Performance Characteristics

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 4900 MHz, TC = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

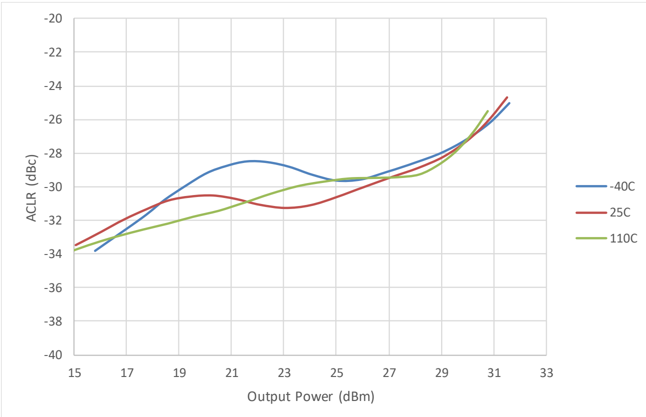


Figure 3. ACLR vs. Output Power Over Temperature (PAR = 8.5 dB, 100 MHz Signal)

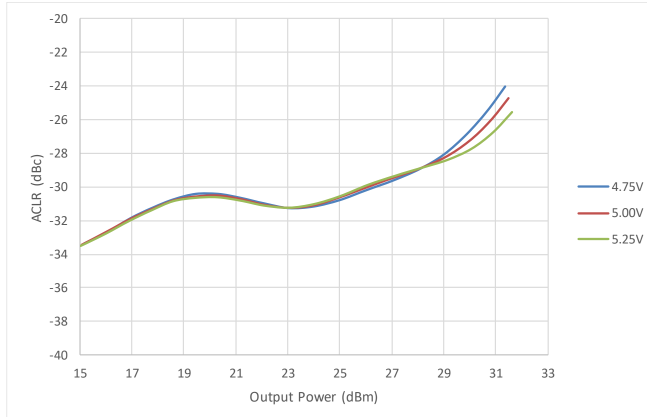


Figure 4. ACLR vs. Output Power Over Voltage (PAR = 8.5 dB, 100 MHz Signal)

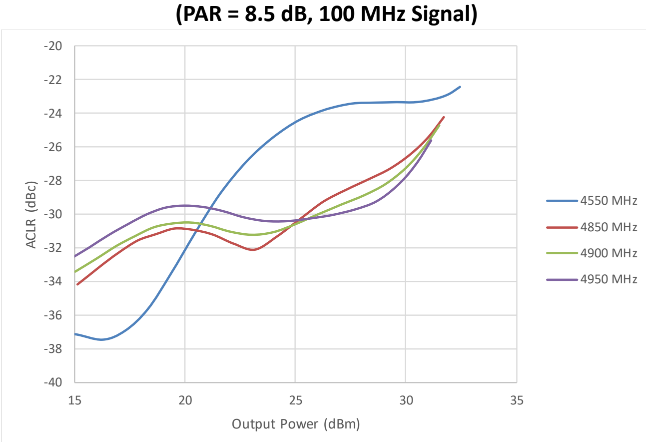


Figure 5. ACLR vs. Output Power Over Freq (PAR = 8.5 dB, 100 MHz)

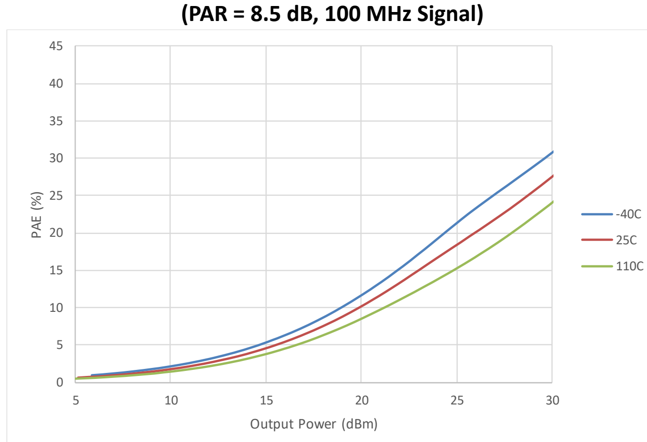


Figure 6. PAE vs. Output Power Over Temperature

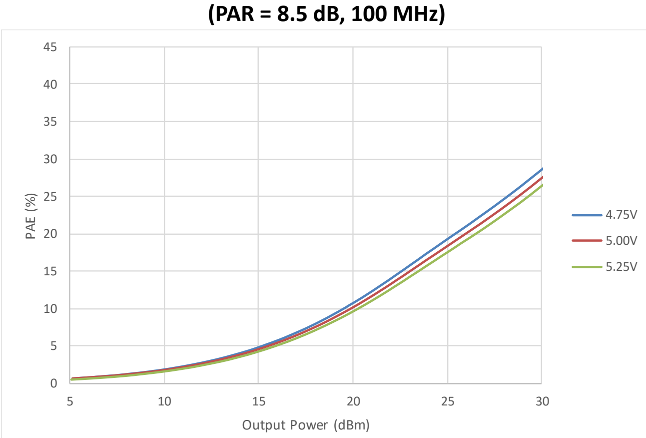


Figure 7. PAE vs. Output Power Over Voltage

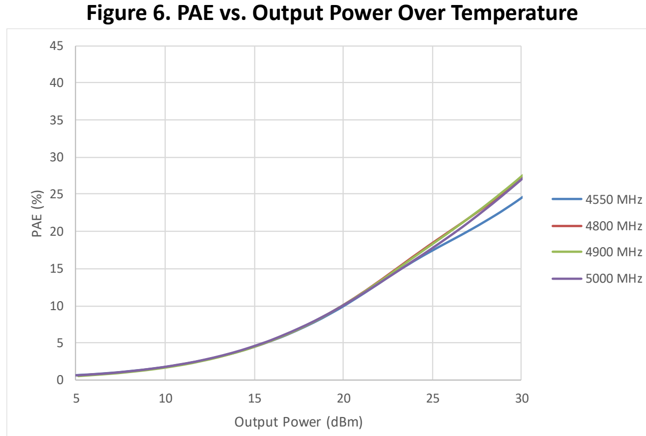


Figure 8. PAE vs. Output Power Over Frequency

Typical Performance Characteristics

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 4900 MHz, TC = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

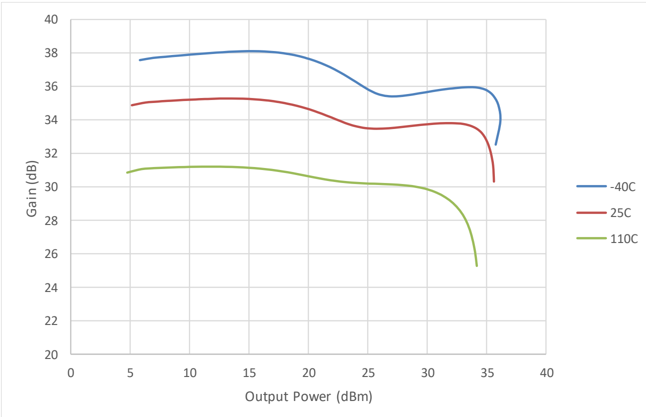


Figure 9. Gain vs. Output Power Over Temperature

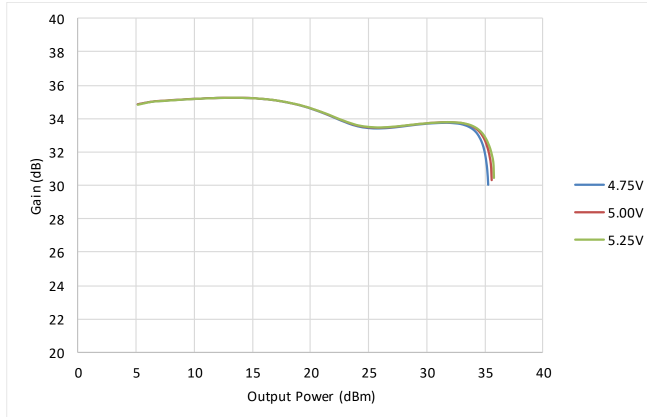


Figure 10. Gain vs. Output Power Over Voltage

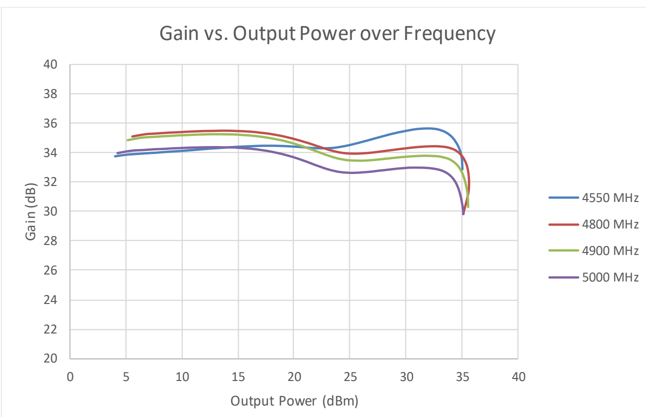


Figure 11. Gain vs. Output Power Over Frequency

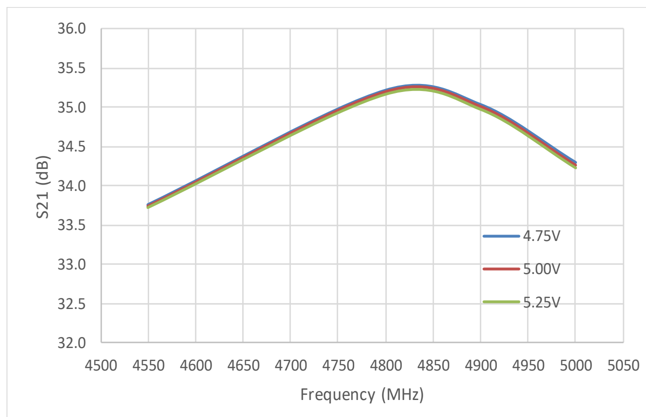


Figure 12. Small Signal Gain Over Voltage

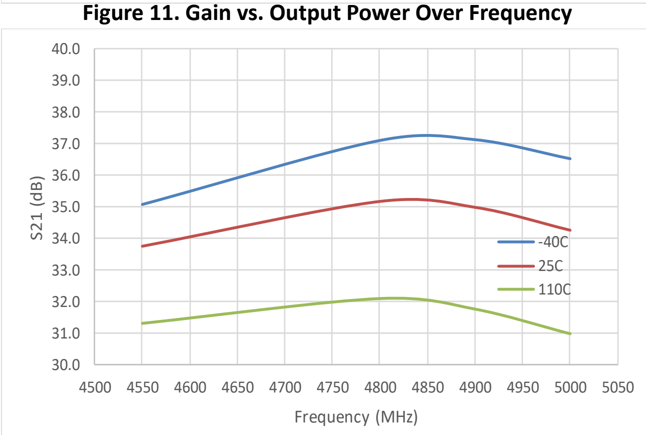


Figure 13. Small Signal Gain Over Temperature

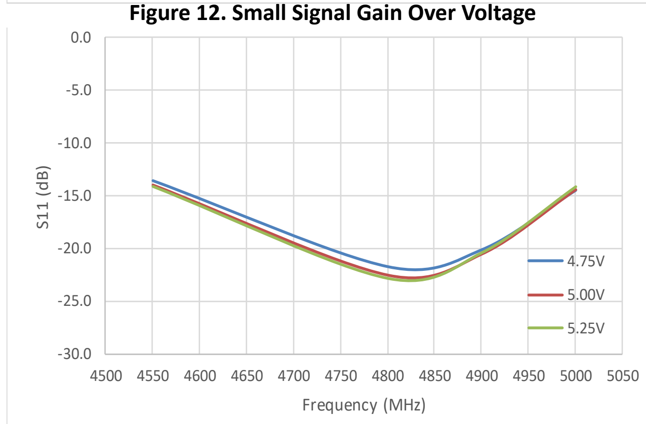


Figure 14. Input Return Loss Over Voltage

Typical Performance Characteristics

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 4900 MHz, TC = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

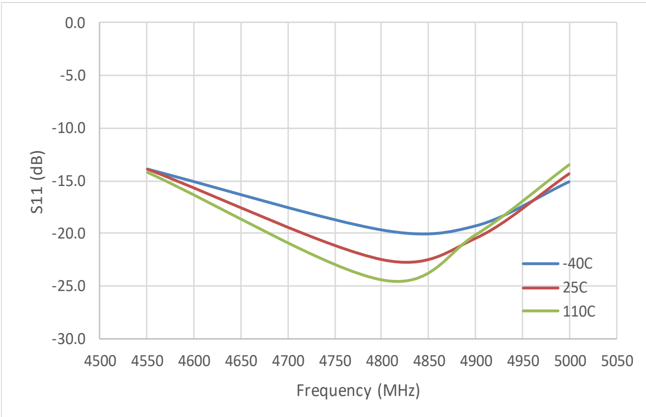


Figure 15. Input Return Loss Over Temperature

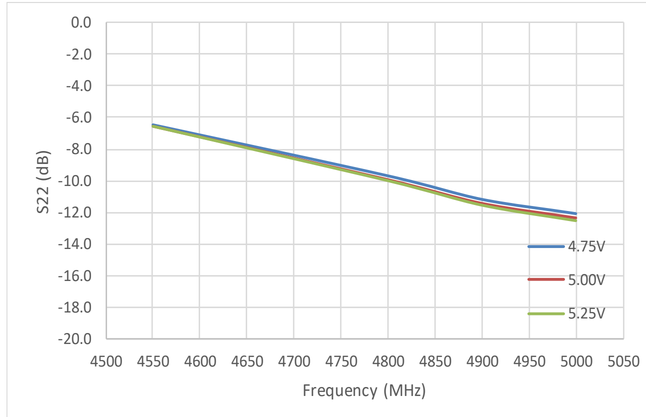


Figure 16. Output Return Loss Over Voltage

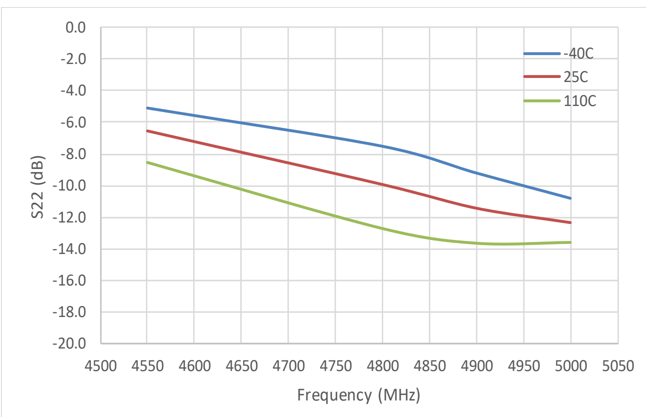


Figure 17. Output Return Loss Over Temperature

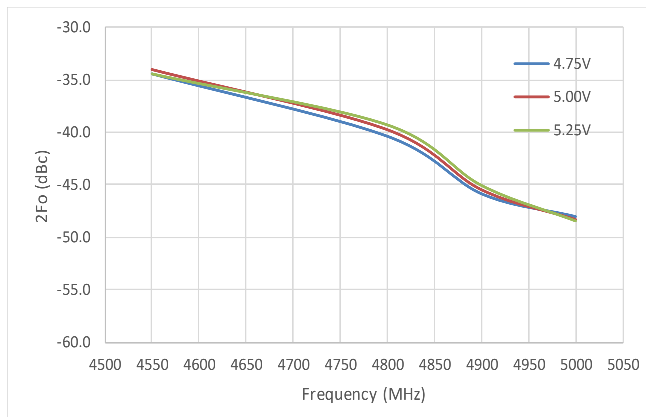


Figure 18. 2nd Harmonic vs. Frequency Over Voltage

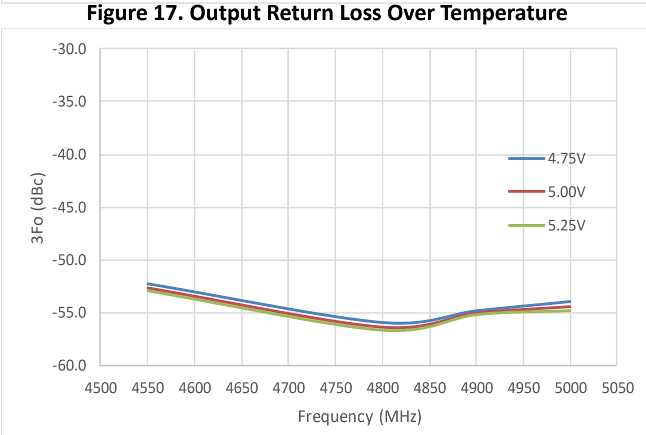


Figure 19. 3rd Harmonic vs. Frequency Over Voltage

Evaluation Board Description

An evaluation board is used to test the performance of the SKY66319-11. An application schematic is provided in Figure 20. Table 6 provides the Bill of Materials list for Evaluation Board components. An assembly drawing, board layer details and physical characteristics follow below.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66319-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.
  Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: A poor connection between the ground pad and ground increases junction temperature (TJ), which reduces the life of the device.

Evaluation Board Test Procedure

Turn-On Sequence

1. Connect 50 ohm test equipment or load to the input and output RF ports of the evaluation board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at -30 dBm and observe that the gain of the device is approximately equal to the gain in Table 5. Begin measurements.

Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

NOTE: It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

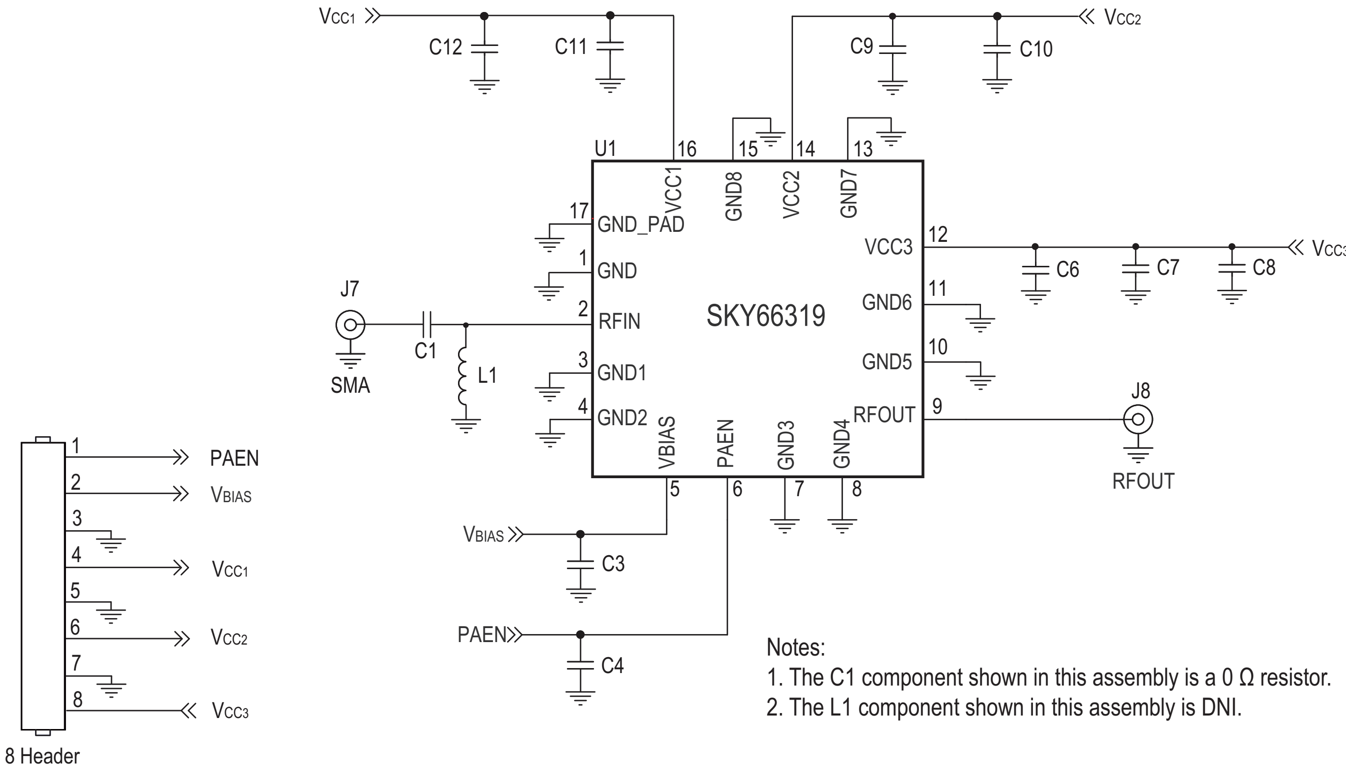
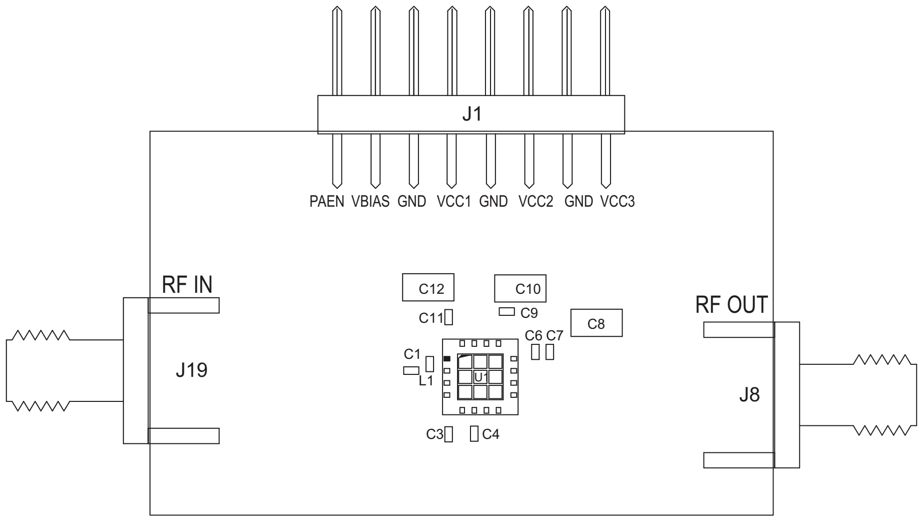


Figure 20. Application Schematic

Table 6. Evaluation Board Bill of Materials

Component	Description	Size
C1	Resistor, 0 ohm, 0.063 W	0402
C3	Ceramic capacitor, 1 uF, ±10%, 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, ±10%, 50 V	0402
C6	Ceramic capacitor, 1 uF	0402
C8, C10, C12	Ceramic capacitor, 10 uF, X7R, ±10%, 16 V	1206
C9	Ceramic capacitor, 0.47 uF	0402
C11	Ceramic capacitor, 0.1 uF	0402
L1	DNI	
TW21-D690-XXXX	Evaluation board	



Notes:
1. Evaluation Board Gerber files are available on request.
2. The C1 component shown in this assembly is a 0 W resistor.
3. The L1 component shown in this assembly is DNI.

Figure 21. Evaluation Board Assembly Drawing

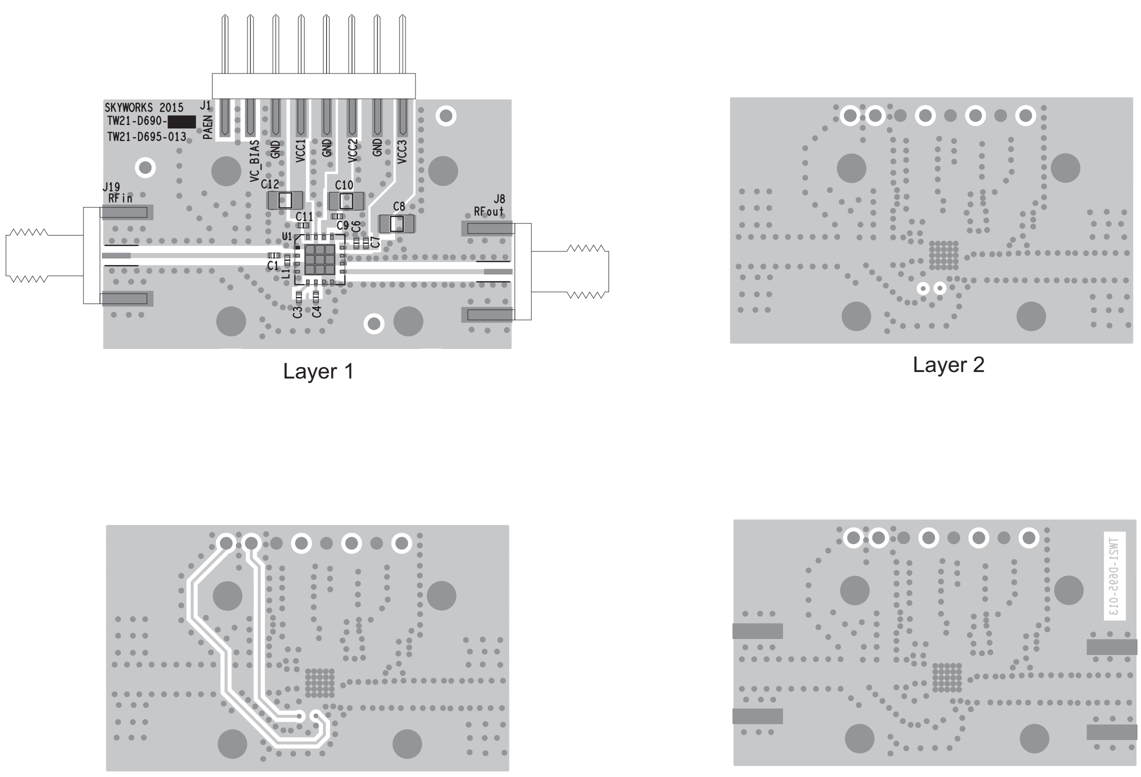


Figure 22. Board Layer Detail

50 Ohm	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

Figure 23. Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

GND (pins 1, 3, 4, 7, 8, 10, 11, 13, 15). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

VBIAS (**pin 5**). The bias supply voltage for each stage, nominally set to +5 V.

RFOUT (**pin 9**). Amplifier RF output pin (ZO = 50 ohms). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.

VCC1, **VCC2**, and **VCC3** (**pin 16**, **15**, and **12**, respectively). Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders and should be populated with 0 ohm resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RFIN (**pin 2**). Amplifier RF input pin (ZO = 50 ohms). All impedance matching is provided internal to the module.

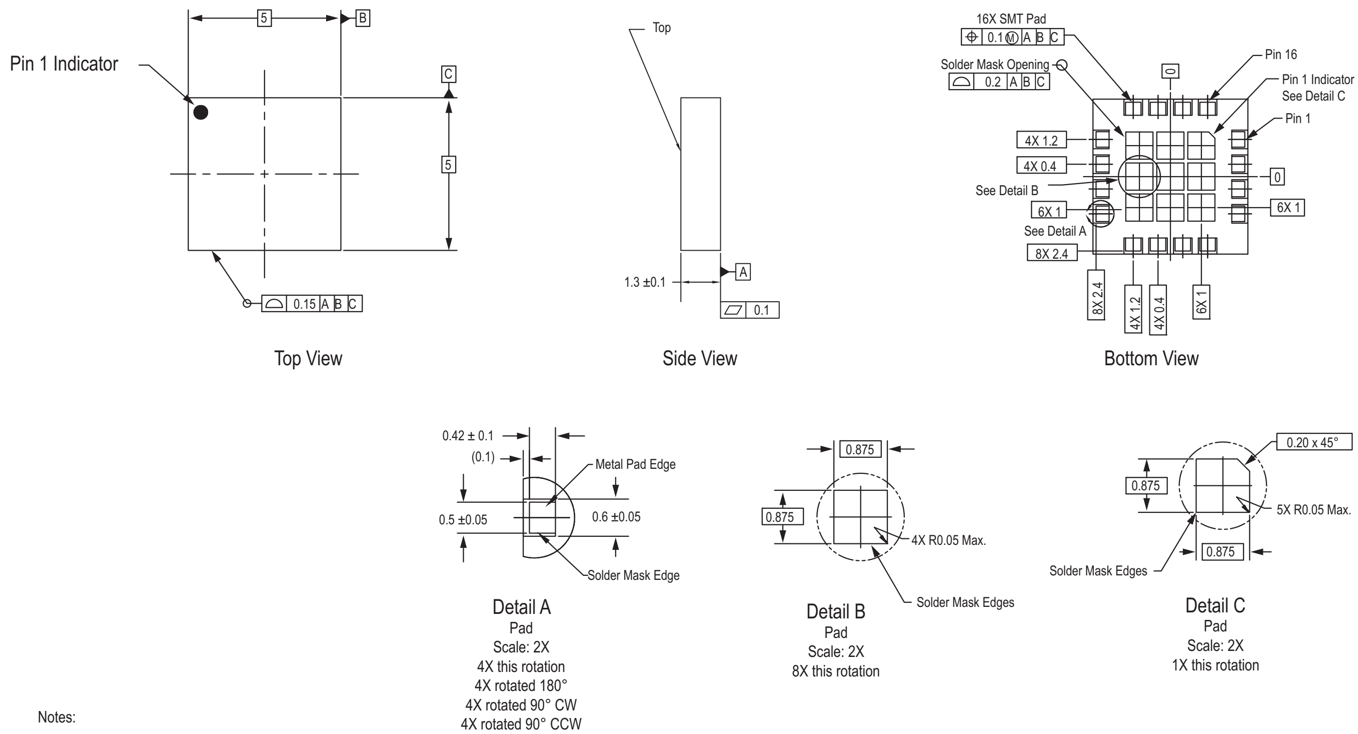
Package and Handling Information

Package dimensions appear below, followed by the PCB layout pattern, typical part marking, and tape and reel information.

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed.

Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly. The SKY66319-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering.

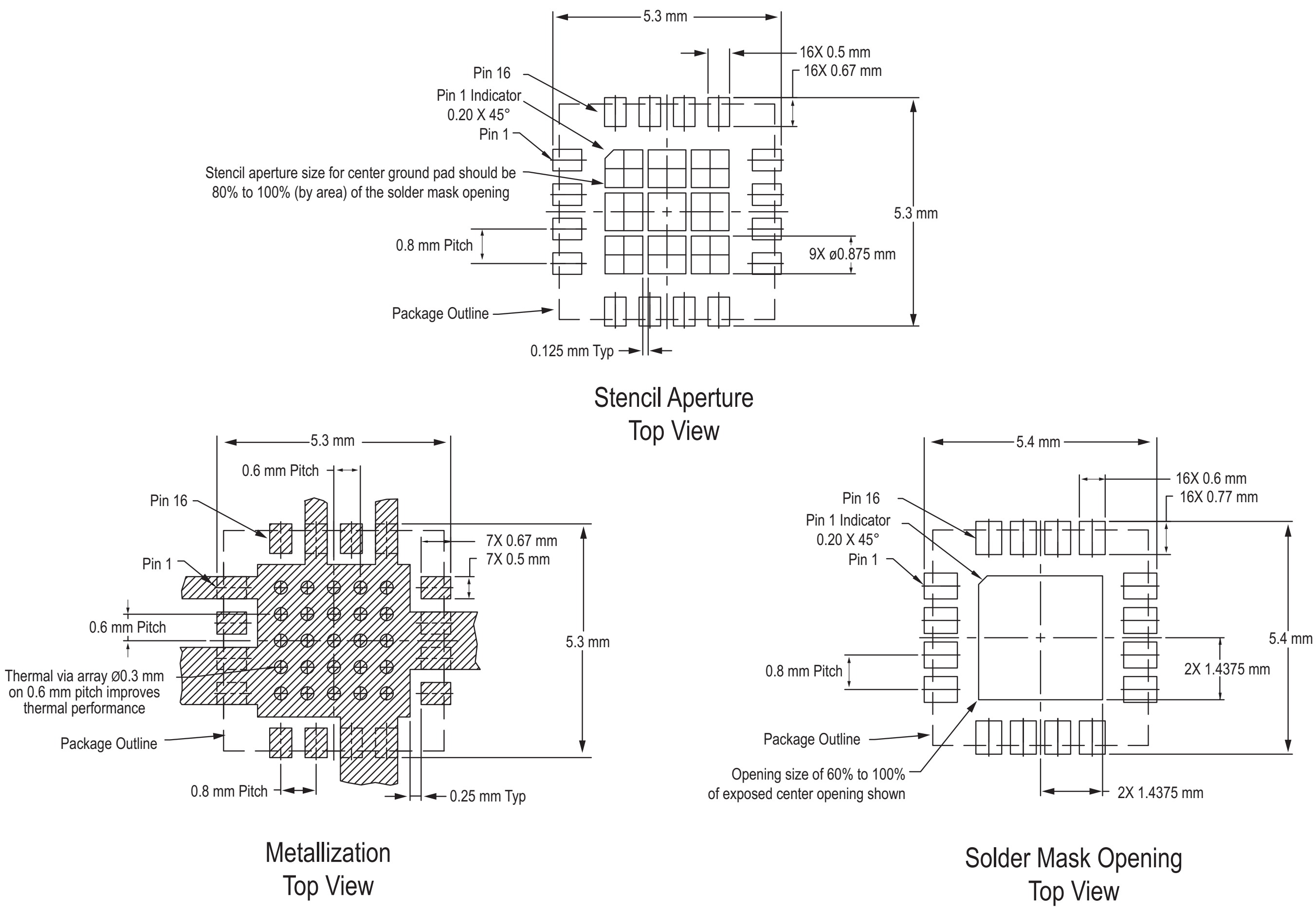
Production quantities of this product are shipped in a standard tape and reel.



Notes:

1. Dimensions are in millimeters (unless otherwise specified).
2. Dimensions and tolerances are in accordance with ASME Y14.5M–1994.

Figure 24. Package Dimensions



Notes:

1. Thermal vias should be resin filled and capped in accordance with IPC–4761 type VII vias.
2. Recommended Cu thickness is 30 to 35 µm.

Figure 25. PCB Layout Diagram

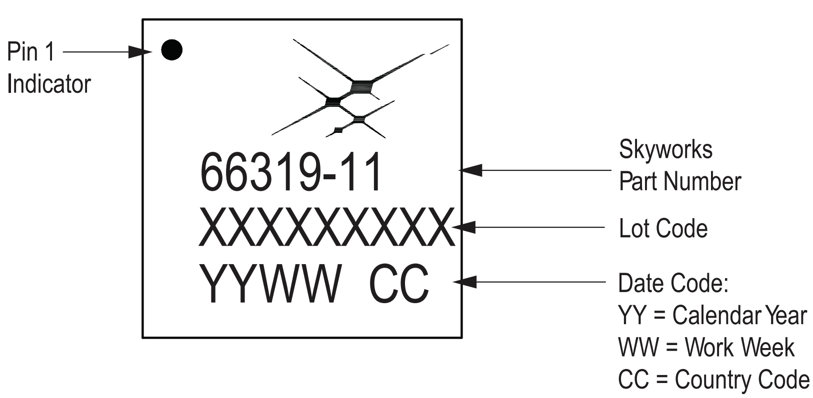
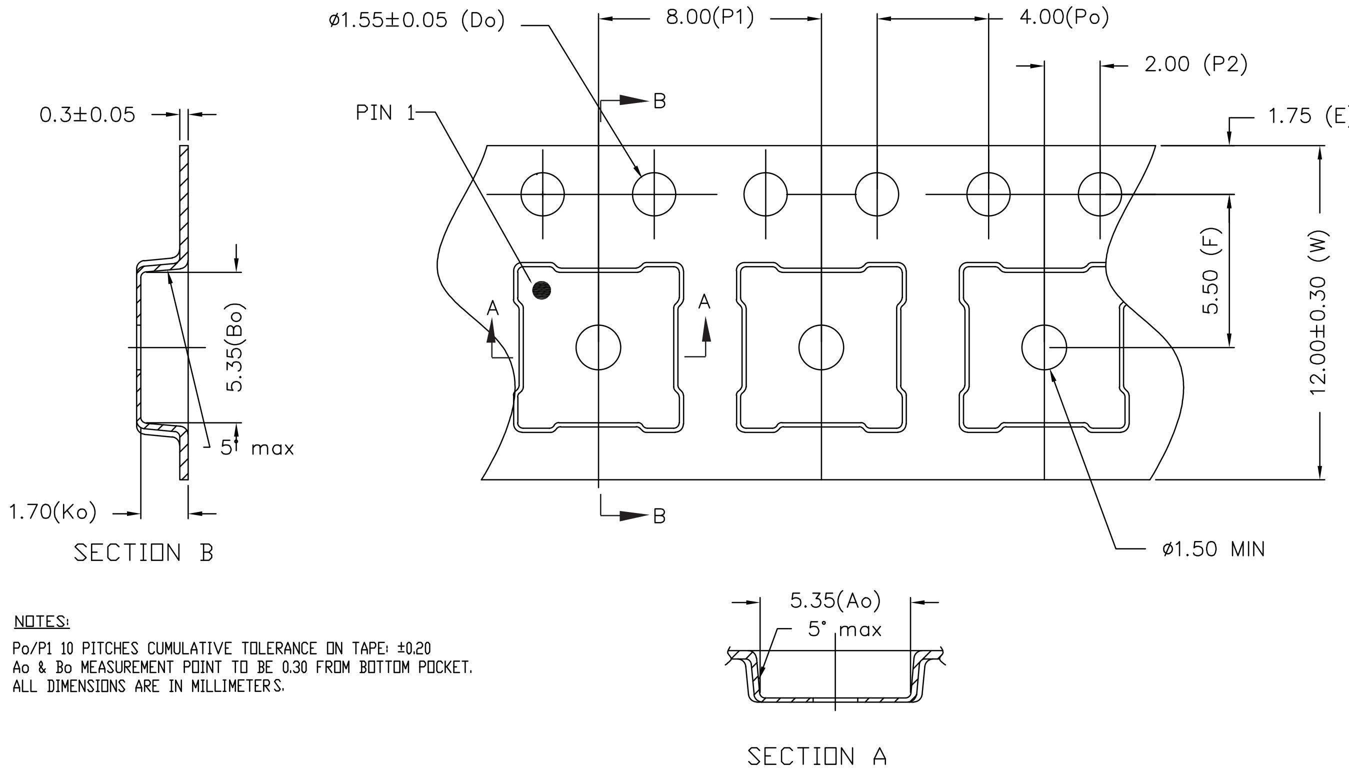


Figure 26. Typical Part Marking



NOTES:
Po/P1 10 PITCHES CUMULATIVE TOLERANCE ON TAPE: ±0.20
Ao & Bo MEASUREMENT POINT TO BE 0.30 FROM BOTTOM POCKET.
ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 27. Tape and Reel Dimensions

Ordering Information

Part Number	Part Description	Evaluation Board Part Number
SKY66319-11	4400 to 5000 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier	SKY66319-11EK1